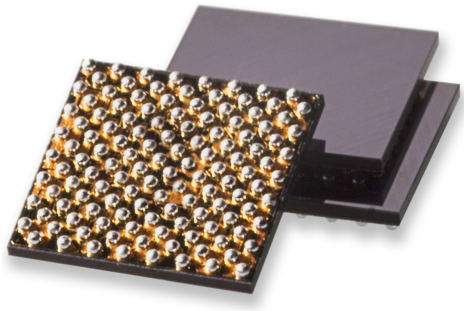
eWLCSP

Encapsulated Wafer Level Chip Scale Package

A compelling value proposition over standard WLCSP, this innovative encapsulated WLCSP technology offers the combined benefits of superior quality, lower cost structure and ease of conversion through drop-in replacement.



Highlights

- Innovative FlexLine™ manufacturing approach delivers compelling cost reductions over standard WLCSP
- Seamless conversion between fan-in and fan-out designs with the same basic package platform
- Unique WLP manufacturing approach independent of incoming silicon wafer diameter

Features

Process

- Wafer agnostic process normalises wafer diameter to uniform processing size making incoming wafer size irrelevant
- All processing performed in wafer form before dicing
- eWLCSP structure identical to conventional WLCSP with exception of protective sidewall coating
- Final back grind thins the package to desired thickness
- Backside surface can be covered with mold compound, exposed with grind process or laminated with protective film
- Standard photolithography; Plated Cu RDL, Plated Cu UBM
- At least 30µm routing space at package edge compared to Si WLCSP
- Typical body thickness: ~300µm
- Same body sizes available as WLCSP (qualified up to 6x6mm); eWLCSP die size can be scaled beyond 6x6mm
- Ball pitch 0.50mm, 0.40mm, 0.35mm
- Fan-out panel/wafer level test before dicing
- Package singulation without touching Si after testing

Quality

- Polymer sidewall offers mechanical protection from die chipping, cracking and other handling issues
- >50% increase in die strength over traditional WLCSP structures
- Advanced dielectrics provide equal/better reliability and performance
- Benefits optimal for larger WLCSP die sizes
- Passes standard CLR, BLR, temperature cycle on board (TCoB) and drop test (equivalent to WLCSP)

Cost

- Drop-in replacement offers low risk, seamless conversion path from standard WLCSP
- Increased savings as panel sizes increase
- FlexLine process qualified at advanced silicon nodes down to 22/20nm

Robust Fan-in WLP Solution

Customers with robust reliability requirements have the option of encapsulating the back and four sidewalls of a WLCSP die. This provides mechanical robustness and resistance to chipping, cracking and handling damage, enabling improved long term reliability over traditional bare die WLCSP. Encapsulation also provides significant structural protection for advanced node products where the die is very thin and dielectric layers are extremely fragile.

Utilizing our FlexLine™ manufacturing approach, we offer an innovative encapsulated WLCSP technology called eWLCSP. With eWLCSP, the formation of a protective polymer coating on the back and four sides of the die surfaces is accomplished using the same high volume reconstitution and wafer level molding process that is used for our Fan-out wafer level technology known as embedded Wafer Level Ball Grid Array (eWLB).

eWLCSP provides a measurable increase in overall component break strength of more than 50% over traditional bare die WLCSP structures which are regularly exposed to potential cracking, chipping and handling issues that can occur before or during the SMT assembly process, especially in advanced node products where the die is very thin and dielectric layers are extremely fragile.

Ease of Conversion, Lower Costs

An additional benefit of our FlexLine manufacturing process is the ease of conversion from a standard WLCSP to an eWLCSP design. Customers can seamlessly transition from a fan-in to fan-out design within the same basic package platform. A product currently using a conventional WLCSP process can be converted to eWLCSP without a silicon design change, regardless of the current silicon wafer diameter. 300mm devices transitioning to advanced silicon nodes with fragile dielectric layers will especially benefit from conversion to eWLCSP.

The FlexLine method can reduce WLCSP costs by 15-30% when using the optimum design requirements for WLCSP devices; e.g., 200mm incoming wafers can be reconstituted into 300mm or larger panel sizes, providing customers with the advantage of panel size scaling.

Process Highlights

Passivation	1 via size: 20µm (minimum)
RL Line/Space	8µm line/8µm space (minimum)
Bump Pitch	0.50mm, 0.4mm, 0.35mm, 0.3mm
Visual Inspection	Automatic optical inspection with electronic wafer mapping

Test Services

Wafer level testing is an important process for yield enhancement and a final test requirement for eWLCSP. Our best-in-class test services include:

- Product Engineering support
- Probe capability
- Program generation/conversion
- High volume wafer sort

Applications

eWLCSP is a compelling solution for space constrained mobile devices and new applications such as wearable technology and automotive markets. Effective transition to eWLCSP is optimal for the following applications:

- 200mm WLCSP migration to FlexLine for PMIC and MCU applications
- 300mm WLCSP migration to eWLCSP for amplifiers, MCU, PMIC and RFIC applications

Component Level Reliability Testing

Moisture Sensitivity Level	MSL1, (260°C, 3x)
Temperature Cycling after Precon	-55°C/125°C, 1000 cycles
Unbiased HAST after Precon	130°C/85% RH, 192 hrs
High Temperature Storage	150°C, 1000 hrs
Temperature Humidity Bias Test	85°C/85%/5V, 1000 hrs
Ball Shear Test	Post reflow: T0, 5X and 10X; reflow: 260 +0/-5 °C

Board Level Reliability Testing

TC on Board (Condition B)	-40°C/125°C, 2 cycles/hr, 500 cycles
Drop Test	Passed JEDEC drop test

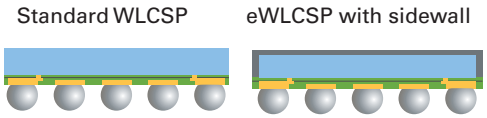
Thermal Performance

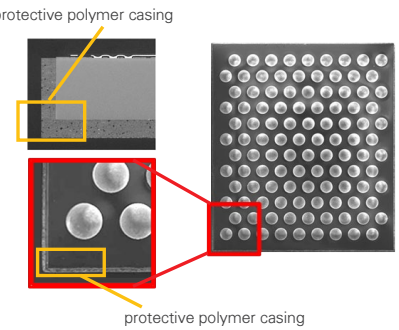
- Thermal performance in the 20-40 C/W range for a 5mm x 5mm die without thermal enhancement
- Application specific thermal characterization available upon request

Electrical Performance

- Dependent on application design, and capable to beyond 10GHz
- Application specific electrical characterization available upon request
- Thick Cu for high current low inductance applications

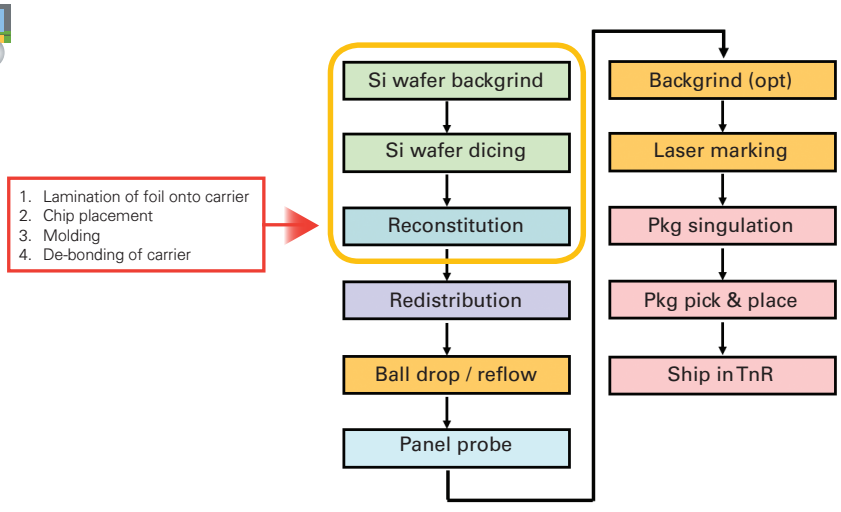
Cross Sections *(Not to scale)*





Encapsulation offers sidewall protection

FlexLine™ Process Flow



The FlexLine process flow leverages the eWLB Fan-Out package process

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