WLCSP

Wafer Level Chip Scale Package

Wafer Level Chip Scale Packaging (WLCSP) is a Fan-in wafer level package (FIWLP) that provides significant package footprint reductions, lower cost, improved electrical performance, and a relatively simpler construction over conventional wirebond or interposer packaging technologies.

Highlights

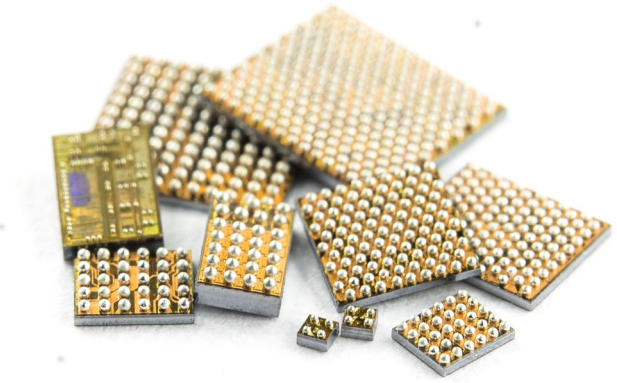
- 200mm & 300mm wafer bumping offers advanced technology in WLP services that enable higher current densities & increased reliability
- Repassivation, Redistribution, Bumping and IPD layer options available
- Full turnkey wafer bumping & Flip Chip-in-Package assembly capability

Features

- WLCSP body sizes qualified up to 6x6mm
- Ball count ranges depending on pitch size and up to 300mm
- Die services available for 8"-12" wafers
- In-house thin film on wafer processing & bumping
- Full service wafer bumping with Polyimide or PBO dielectric options for wafer repassivation, redistribution and IPD layers
- Bumps formed by printed paste, electroplate or ball drop solder bump technologies
- Minimum available flip chip bump pitch of 150µm
- Large bump (220-500µm) processing at 0.35mm pitch & greater for Flip Chip-on-Board & WLCSP applications
- For larger pitch applications, either printed paste bumping or mechanical ball drop available
- Eutectic and Pb-free solder
- Copper under bump metallization (UBM) & redistribution layers (RDL) available
- Wafer level IPD & thick copper (8-12µm) conductors available
- Underfilling of substrate mounted bumped die may or may not be required depending on customer's specific application & reliability requirements
- Underfilling by overmolding is feasible
- Low cure temperature polymers available
- Flexible bare die processing
- Compatible with conventional SMT assembly and test techniques

Applications

A small, lightweight, high performance semiconductor solution, WLCSP is a compelling, cost effective solution for space constrained mobile applications and other portable consumer and industrial devices.

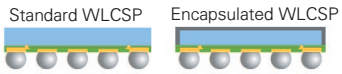


Compact Packaging Solution

As a small, lightweight, high performance semiconductor solution, Wafer Level Chip Scale Packaging (WLCSP) is a Fan-in wafer level package (WLP) that offers compelling advantages for cost and space constrained mobile devices and new applications such as wearable electronics. With WLCSP, all of the manufacturing process steps are performed in parallel at the silicon wafer level rather than sequentially on individual chips to achieve a package that is essentially the same size as the die. WLCSP has dielectrics, thin film metals, and solder bumps directly on the surface of the die, achieving in a final package that is no larger than the required circuit area. WLCSP solutions provide significant package footprint reductions, lower cost, improved electrical performance, and a relatively simpler construction over conventional wirebond or interposer packaging technologies.

Protective Sidewall Coating

Customers with robust reliability requirements have the option of encapsulating the back and four sidewalls of the die. This provides mechanical robustness and resistance to chipping, cracking and handling damage, enabling improved long term reliability over traditional bare die WLCSP. Encapsulation also provides significant structural protection for advanced node products where the die is very thin and dielectric layers are extremely fragile.



We offer two types of Fan-in WLP with protective sidewall coating: encapsulated Wafer Level Chip Scale Packaging (eWLCSP) and Fan-in Embedded Chip Package (FI-ECP). With eWLCSP, the formation of a protective polymer coating on the back and four sides of the die surfaces is accomplished using the same high volume reconstitution and wafer level molding process that is used for our Fan-out wafer level technology known as embedded Wafer Level Ball Grid Array (eWLB). Since the majority of WLCSP products use 200mm wafers, reconstitution enables the scaling of eWLCSP on 200mm wafers to 300mm or high density carrier sizes for processing. FI-ECP has a similar package structure, but follows a different manufacturing flow based on plasma dicing and the lamination process.

Process Highlights

Die Thickness	8" 200-760mm (8-30mils) 12" 250-790mm (10-32mils)
Bumped Die Height	0.3mm minimum; 0.40mm and 0.80mm standard
Printed Bump Height	70nm
Solder Sphere Diameter	250mm ball drop
Bump Pitch	0.5mm, 0.4mm, 0.35mm and 0.3mm
Redistribution	10µm lines, 10µm spaces
Visual Inspection	Automatic optical inspection with electronic wafer mapping

Standard Materials

Dielectric Material	Polyimide & PBO
RDL	Sputtered AlCu, Plated Cu
UBM	AlCu/NiV/Cu, Ti/NiV/Cu, Plated Cu
Solder Alloy	Eutectic (standard and ultra-low alpha) including Pb-free SAC 405, 305 or 105 (95.5Sn/4.0Ag/0.5Cu, 96.5Sn/3.0Ag/0.5Cu or 98.5Sn/1.0Ag/0.5Cu)
Ball	Hi Pb, Eutectic, Pb-free; LF35 (available on request)
Electroplate	Hi Pb, Eutectic, Pb-free

Component Level Reliability Testing

Moisture Sensitivity Level	Eutectic printed bump: JEDEC Level 1 @ 220°C Pb-free printed bump: JEDEC Level 1 @ 260°C
Temperature Cycling	-55°C/125°C, 1000 cycles (eutectic & Pb-free printed bumps)
High Temperature Storage	150°C, 1000 hrs (eutectic & Pb-free printed bumps)
Multiple Solder Reflow	5x, 10x and 20x reflows with minimal reduction in bump shear strength
Pressure Cooker Test	121°C/100% RH, 168 hrs

Thermal Performance

- Thermal performance in the 20-40 C/W range for a 5mm x 5mm die without thermal enhancement
- Application specific thermal characterization available upon request

Electrical Performance

- Dependent on application design, and capable to beyond 10GHz
- Application specific electrical characterization available upon request
- Thick Cu for high current low inductance applications

Related Services

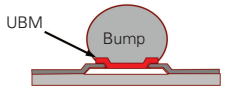
Wafer Thinning	Fully automated backgrinding & mechanical polishing
Backside Coating	Laminated coating
Marking	Laser marking
Packing Options	Fully automated die pick/place into custom pocket tape/reel or waffle pack media

Test Services

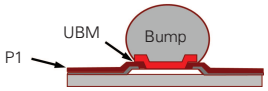
- Product Engineering support
- Probe capability
- Program generation/conversion
- High volume wafer sort

Cross Sections

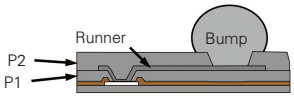
FOC (Bump on I/O)



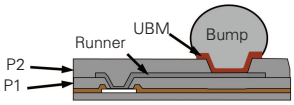
RPV (Repassivation)



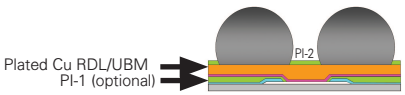
RDL 3M (Redistribution)



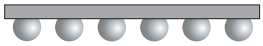
RDL 4M (Redistribution)



Thick Copper RDL (12µm)



WLCSP Bumped Bare Die



STATS ChipPAC Pte. Ltd.
www.statschippac.com or www.jcetglobal.com