

“Encapsulated Wafer Level Package Technology (eWLCSP)

by

**Tom Strothmann, *Seung Wook Yoon, *Yaojian Lin
STATS ChipPAC Inc.1711 W Greentree Drive Tempe, AZ 85284 USA
* STATS ChipPAC Ltd. 5 Yishun Street 23, Singapore 768442
tom.strothmann@statschppac.com**

Copyright © 2014. Reprinted from 2014 Electronic Components and Technology Conference (ECTC) Proceedings. The material is posted here by permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any STATS ChipPAC Ltd’s products or services. Internal or personal use of this material is permitted, however, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or distribution must be obtained from the IEEE by writing to pubs-permission@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

Encapsulated Wafer Level Package Technology (eWLCS)

Tom Strothmann, *Seung Wook Yoon, *Yaojian Lin
STATS ChipPAC Inc. 1711 W Greentree Drive Tempe, AZ 85284 USA
* STATS ChipPAC Ltd. 5 Yishun Street 23, Singapore 768442
tom.strothmann@statschppac.com

Abstract

This paper introduces a new encapsulated WLCSP product (eWLCS). The new product has a thin protective coating applied to all exposed silicon surfaces on the die. The applied coating protects the silicon and fragile dielectrics and prevents handling damage during dicing and assembly operations, effectively providing a durable packaged part in the form factor of a WLCSP. The manufacturing process leverages existing high volume manufacturing methods with exceptionally high process yields. In this process the silicon wafer is diced prior to the wafer level packaging process. The dice are then reconstituted into a new wafer form with adequate distance between the die to allow for a thin layer of protective coating to remain after final singulation. Standard methods are used to apply dielectrics, thin film metals, and solder bumps. The resulting structure is identical to a conventional WLCSP product with the addition of the protective sidewall coating. This paper discusses the key attributes of the new package as well as the manufacturing process used to create it. Reliability data will be presented and compared to conventional WLCSP products and improvements in package durability will be discussed and compared to conventional WLCSP.

Improving the Conventional WLCSP Structure

The wafer level chip scale package was introduced in 1998 as a semiconductor package wherein all packaging operations were done in wafer form [1]. The resultant package has dielectrics, thin film metals, and solder bumps directly on the surface of the die with no additional packaging. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon exposed on the remaining sides and back of the die. The WLCSP is the smallest possible package size since the final package is no larger than the required circuit area. Based on the small form factor and low cost, the number of Wafer Level Packages used in semiconductor packaging has experienced significant growth since its introduction. The growth has been driven aggressively by mobile consumer products because of the small form factor and high performance required in the package design. Although WLCSP is now a widely accepted package option, the initial acceptance of WLCSP was limited by concerns with the SMT assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of the package, however damage to the exposed silicon remains a concern. This is particularly true for advanced node products with fragile dielectric layers. One method commonly used to improve die strength and reduce silicon chipping during assembly is lamination of an epoxy film on the back of the die. The film is

laminated and cured on the back of the wafer prior to singulation to strengthen the die, in spite of the fact it adds cost to the package. By the nature of the backside lamination process, the uncoated sides of the die continue to be exposed after dicing the wafer and the silicon continues to be at risk for chipping, cracking, and other handling damage during the assembly process.

A process has been developed to provide five sided protection for the exposed silicon surfaces in a WLCSP. The process starts with a high volume manufacturing flow developed by STATS ChipPAC for fan-out products. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations [2]. In this manufacturing method the wafer is diced at the start of the process and then reconstituted into a standardized wafer (or panel) shape for the subsequent process steps. The basic process flow for creating the reconstituted wafer is shown in Figure 1. 1) The reconstitution process starts by laminating an adhesive foil onto a carrier. 2) The singulated die are accurately placed face down onto the carrier with a pick and place tool. 3) A compression molding process is used to encapsulate the die with mold compound while the active face of the die is protected. 4) After curing the mold compound, the carrier and adhesive foil are removed in a de-bonding process resulting in a reconstituted wafer where the mold compound encapsulates all exposed silicon die surfaces. The eWLB process is unique since the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes.

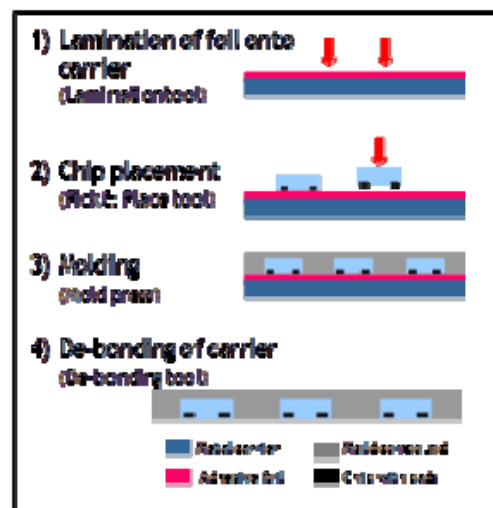


Figure 1. The Reconstitution Process Flow

After the reconstitution process, the reconstituted wafer is processed with conventional wafer level packaging

techniques for the application and patterning of dielectric layers, thin film metals for redistribution and under bump metal, and solder bumps. In the final dicing operation a thin layer of mold compound, typically < 70um, is left on the side of the die as a protective layer. The back of the die is also protected with mold compound, although with a greater thickness. A schematic drawing of a typical structure is shown in Figure 2 for greater clarity. Alternatively, the backside mold compound can be removed and the body made thinner with an optional back grind operation without damaging the protective sidewall layer. The remaining sidewall coating will continue to protect the fragile silicon sides of the die during the assembly operation.

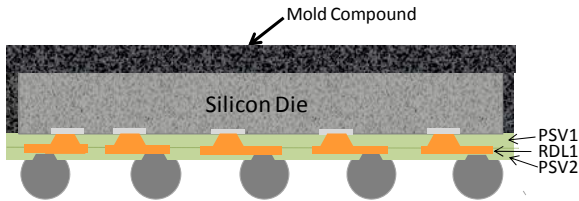


Figure 2. eWLCSP™ Structure

The Encapsulated WLCSP Process

The FO-WLP process has been discussed in many venues and it is recognized as an industry standard process. In the FO-WLP process the area of the package is increased to allow for placement of RDL layers and solder balls outside of the silicon die area [3]. This packaging method allows the die to shrink to a minimum size independent of the required area for an array of solder balls at industry standard BGA ball pitches [4]. It also allows for novel multi-die structures, 2.5D structures and 3D structures [5]. The Fan-out process has been qualified to a 28nm process node with the same dielectrics and Cu plating as are used in the eWLCSP process described here [5]. The eWLCSP process data presented in this paper was generated with a 300mm round reconstituted panel [2]. In the case of conventional FO-WLP the die are typically widely spaced to allow for the expanded RDL and bump area and the conventional saw street. In the case of eWLCSP the die are closely spaced allowing for only the sidewall thickness in addition to a street area of 80um. The die size used this evaluation was 4.5x4.5mm similar to the construction shown in Figure 2. The final structure had 2 layers of polymer and 1 layer of plated Cu RDL with the solder ball mounted directly on the RDL without the use of a separate UBM layer. The process flow used is shown in Figure 3 and the details of the structure are shown in Table 1.

PSV 1 (um)	7.0 - 11.0
RDL 1 (um)	7.0 - 10.0
PSV 2 (um)	7.0 - 11.0
Ball pitch (mm)	0.4
Ball size (um)	250
Solder alloy	SAC 405

Table 1. Layer Thickness

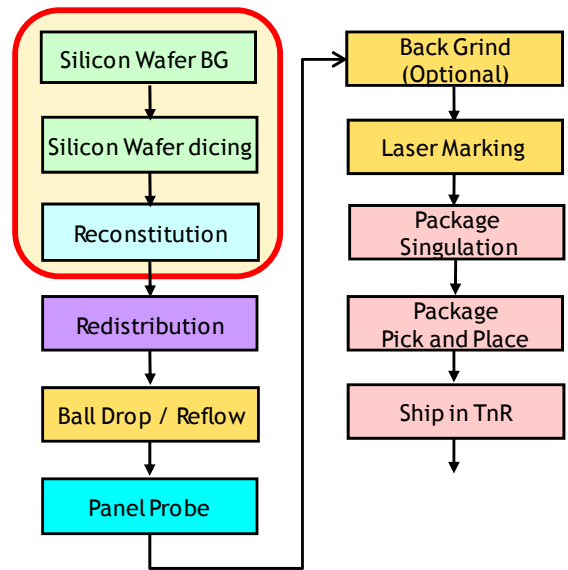


Figure 3. eWLCSP Process Flow

Intuitively the process flow shown in Figure 3 would have higher cost since there are additional steps required for reconstitution at the start of the flow. There are two key factors that offset the cost of the additional steps required for the reconstitution to make this a commercially viable process. 1) Panel size scaling reduces the unit cost if the source silicon wafer is smaller than the reconstituted panel size. In the case of the 300mm reconstituted panel used here the cost is very competitive for silicon wafers with a diameter of 200mm and below. The cost of processing a 300mm reconstituted panel for WLCSP is approximately 1.7x the cost of processing a conventional 200mm silicon wafer in WLCSP, however the units processed per panel increases by a factor of 2.3x, effectively offsetting the cost of reconstitution. 2) Since known good die can be selected at the start of the process, advanced devices that have a lower electrical yield can be tested in wafer form prior to the process. If the incoming wafer has a probe yield of 85%, then 15% more units per reconstituted panel can be processed to offset the cost of the reconstitution process. Since the reconstituted panel size is no longer linked to the incoming silicon wafers size, the panel size can be increased over time and change from a round to a much larger rectangular format. This scaling to a larger panel size will provide a compelling cost reduction when compared to conventional WLCSP packaging methods where the round silicon format is maintained throughout the wafer level packaging process.

One difference in processing panels in the reconstitution flow is found in the attributes of the polymers that are used. In conventional WLCSP either polyimide (PI) or polybenzoxazole (PBO) are used as the dielectrics for planarization, stress buffering and RDL insulation. In the case of the reconstituted panel, the mold compound has a lower temperature threshold than silicon and sustained temperatures over 200°C can cause degradation of the material. PI typically has a cure temperature of 380°C and PBO has a typical cure temperature of 300°C and therefore cannot be used in the

process. A new low temperature polymer has been developed for this application that has a cure temperature compatible with the 200°C threshold temperature of the mold compound.

A SEM cross-section of a eWLCSP part created in the process is shown in Figure 4. In this case a thicker sidewall protection layer was used to demonstrate the process on an existing production device running in the conventional 200mm WLCSP production line. The device demonstrated equivalent electrical yield, Component Level Reliability and Board Level Reliability performance to the conventional WLCSP.

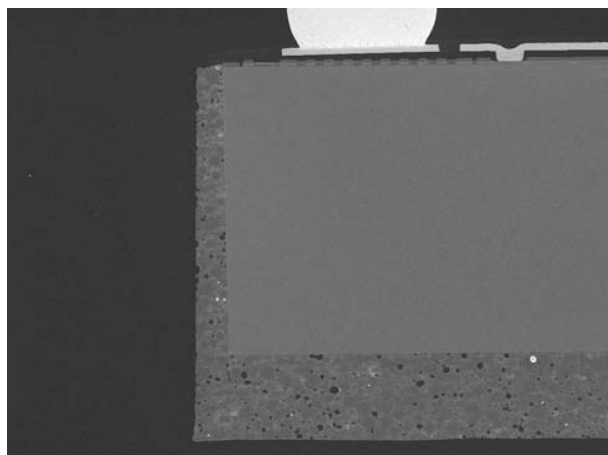


Figure 4. Cross-section of eWLCSP

A second SEM cross-section is shown in Figure 5 showing the finished package with a thin protective sidewall coating and the use of the optional back grind to thin the body thickness.

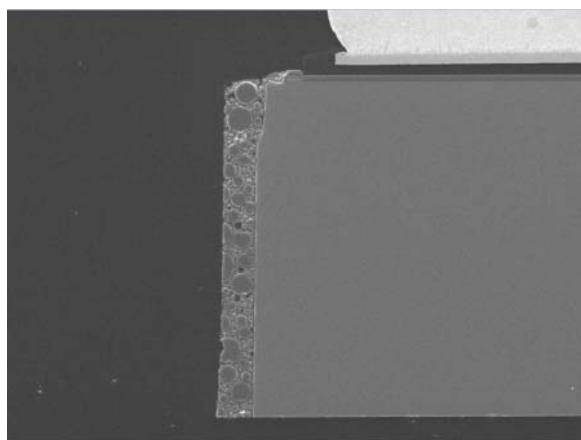


Figure 5. Cross-section of thin body eWLCSP

A WLCSP product that is currently in production using a conventional WLCSP process can be converted to a eWLCSP product without any design change required, regardless of the current silicon wafer diameter. If a reduced thickness is required for the specific application, an optional back grind step can be added to the process flow to reduce the body

thickness while retaining the protective sidewall coating. Since the dice are singulated at the start of the process, the manufacturing equipment and bill of materials are the same for any incoming wafer size. The initial back grind and dicing tools are the only wafer size dedicated equipment required for the process. Very little process development and very little additional capital will be required to package 450mm silicon wafers as eWLCSP.

eWLCSP Product Assessment

The unique attribute of the eWLCSP package is the protective sidewall coating. The protective layer is durable and will prevent silicon chipping on the side of the package. This protective layer has the ability to protect the silicon during socket insertion for test. This has been demonstrated through multiple insertion test on completed products with no observed damage to the protective coating.

The eWLCSP process has passed standard reliability tests used in wafer level packaging including Component Level Reliability (CLR), Temperature Cycle on Board (TCoB), and Drop Test.

Component Level Reliability was completed with the test conditions shown in Table 2. The evaluation results were confirmed by visual inspection and electrical test. No delamination of the protective coating was detected during the CLR evaluation.

Component Level Test	Condition		Status
MSL1	MSL1, 260C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55°C to 125°C	1000 x	Pass
HAST (w/o bias) after Precon	130°C / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150°C	1000 hrs	Pass

Table 2. Component Level Reliability Results

Thermal Cycle Reliability Test (TCoB) was completed and passed 500 cycles with the results shown in Table 3 and the Weibull plot in Figure 6. Results were obtained from electrical measurement of daisy chain bump structures. Results are comparable to conventional WLCSP product produced with polyimide dielectrics.

TCoB (Cond B)	Failure Rate	Characteristic life (η)	Weibull slope (β)	First Failure
-40°C to 125°C	0.635	1219.4	10.13	864x

Table 3. TCoB Reliability Test Results

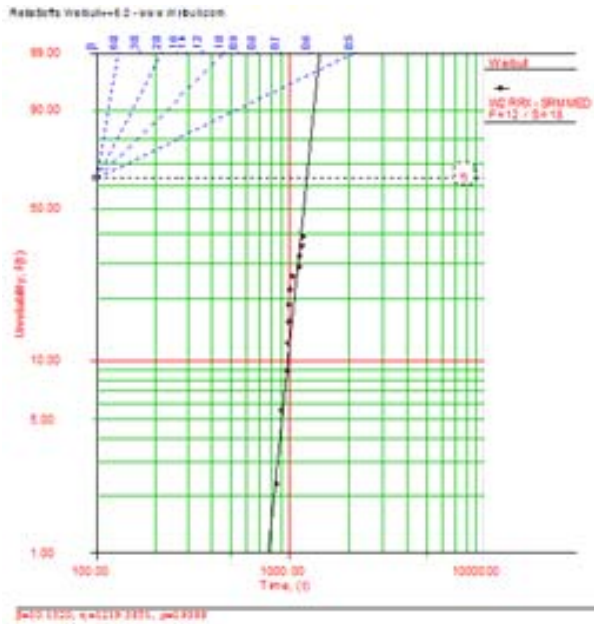


Figure 6. TCoB Weibull Plot for eWLCSP

Drop Test was completed and passed the JEDEC requirement of 30 drops with the results shown in Table 4 and the Weibull plot in Figure 7. Results were obtained from electrical measurement of daisy chain bump structures. Results are comparable to conventional WLCSP product produced with polyimide dielectrics.

Drop Test	Failure Rate	Characteristic life (η)	Weibull slope (β)	First Failure
JEDEC	0.635	1553.5	5.97	772x

Table 4. Drop Test Results for eWLCSP

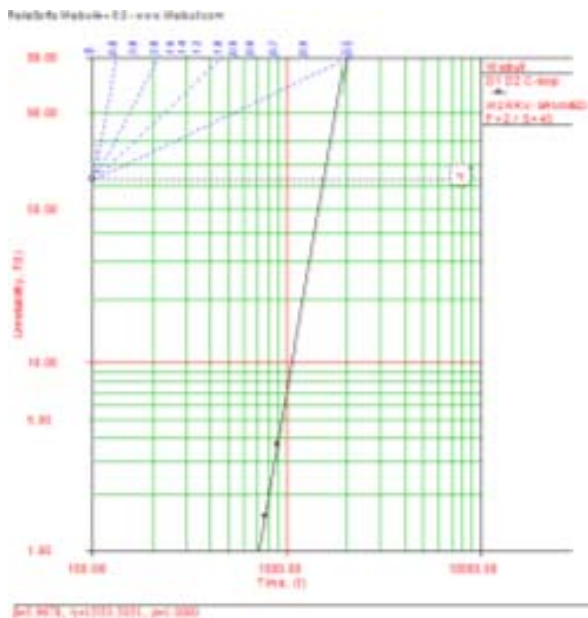
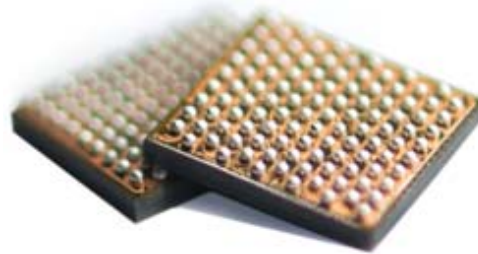


Figure 7. Drop Test Weibull Plot for eWLCSP

Conclusions

A new encapsulated WLCSP process has been developed and verified with reliability testing. The process provides mechanical sidewall protection to WLCSP parts with an increase in package size of less than 100um in X and Y dimensions. The sidewall protection resolves the problem of silicon damage during the assembly process and provides a path to significant cost savings for the customers as the panel size is increased. The eWLCSP process described is wafer size agnostic, so the same manufacturing line can process the eWLCSP products regardless of the incoming wafers size. 450mm wafers can easily be accommodated for the encapsulated WLCSP process once the service is required by the customers.



eWLCSP Product with Protective Sidewall Coating

Acknowledgments

STATS ChipPAC WP/eWLB development team supporting WLP Research and Development.

References

1. P. Elenius, "The Ultra CSP Wafer Scale Package", Electronics Packaging Technology Conference, 1998.
2. M. Prashant, S.W. Yoon, Y.J. Lin, and P.C. Marimuthu, "Cost effective 300mm large scale eWLB (embedded Wafer Level BGA) Technology", 2011 13th Electronics Packaging Technology Conference.
3. M. Brunnbauer, et al., "Embedded Wafer Level Ball Grid Array (eWLB)," Proceedings of 8th Electronic Packaging Technology Conference, 2009, Singapore (2006)
4. M. Brunnbauer, T Meyer, "Embedded Wafer Level Ball Grid Array (eWLB)," IMAPS Device Packaging Conference 2008, Arizona, US
5. SW Yoon, P Tang, R Emigh, YJ Lin, PC Marimuthu, R Pendse, "Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions", 2013 Electronic Components & Technology Conference.