PBGA-SD
Plastic Ball Grid Array - Stacked Die

Highlights

- Stacking of die enables more functionality and integration in a conventional PBGA package

Features

- Increased sub-system performance achieved by integrating multiple chips into a single package
- Die to die bonding capability for device/signal integration
- 15 x 15mm to 40 x 40mm body sizes available
- Ball counts up to >1000 balls
- 0.65, 0.80, 1.00, 1.27 and 1.5mm ball pitch
- SnPb and Pb-free balls available
- Full in-house design capability with wide range of custom and open tool designs
- Full in-house electrical, thermal and mechanical simulation and measurements capability
- Multiple chip design and optional passive/discrete components available
- Standard 2, 4 and 6 layer substrates as well as high density substrate options
- Pb-free and green material set options
- Multiple routing layers and dedicated ground/power planes available for improved electrical and thermal performance

Description

BGA packages can be used for high performance applications with high I/O connections and high thermal and electrical requirements. The characteristics of BGA packages make them suitable for a wide variety of devices used in computing platforms, networking, hand-held consumer products, wireless communications devices, video cameras, home electronic devices and game consoles.

Our chip stack technology offers the flexibility of stacking 2 to 7 die in a single package. The Stacked Die Plastic Ball Grid Array (PBGA-SD) package takes advantage of the proven high electrical and thermal performance of PBGA packages, with efficient use of space made possible through die stacking technology. PBGA-SD packages use laminate substrates and are available in a variety of body sizes and ball counts, combining advanced assembly processes and proven material sets for enhanced yield, reliability and performance.

Applications

- DSPs and Memory
- Gate Arrays
- ASICs
- PC Chipsets and Peripherals
- Microprocessors/Controlers
Specifications

Die Thickness 150-381µm (6-15mils)
Gold Wire 15-30µm (0.6/0.7/0.8/0.9/1.0/1.1/1.2mils) diameter
Pd/Cu Wire 15-30µm (0.6/0.7/0.8/1.0mils) diameter
Bond Pad Pitch 45µm inline or 25/50µm staggered capable
Mold Cap Thickness 0.7-1.17mm
Marking Laser
Packing Options JEDEC tray/tape & reel

Reliability

Moisture Sensitivity Level JEDEC Level 3, 260°C reflow
Temperature Cycling Condition C (–65°C/150°C), 1000 cycles (typical)
High Temperature Storage 150°C, 1000 hrs (typical)
Pressure Cooker Test 121°C, 100% RH/2 atm, 168 hrs
Temperature/Humidity Test 85°C/85% RH, 1000 hrs
Unbiased HAST 130°C/85%, RH/2 atm, 96 hrs

Thermal Performance θja (°C/W)

The thermal performance of each die in the stack is influenced by other die in the stack. Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed.

Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

<table>
<thead>
<tr>
<th>Conductor Component</th>
<th>Length (mm)</th>
<th>Resistance (mOhms)</th>
<th>Inductance (nH)</th>
<th>Inductance Mutual (nH)</th>
<th>Capacitance (pF)</th>
<th>Capacitance Mutual (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire</td>
<td>2</td>
<td>120</td>
<td>1.65</td>
<td>0.45 - 0.85</td>
<td>0.10</td>
<td>0.01 - 0.02</td>
</tr>
<tr>
<td>Net (2L)</td>
<td>2 - 7</td>
<td>34 - 119</td>
<td>1.3 - 4.55</td>
<td>0.26 - 2.28</td>
<td>0.25 - 0.95</td>
<td>0.06 - 0.42</td>
</tr>
<tr>
<td>Total (2L)</td>
<td>154 - 239</td>
<td>2.95 - 6.2</td>
<td>0.71 - 3.13</td>
<td>0.35 - 1.05</td>
<td>0.07 - 0.44</td>
<td></td>
</tr>
<tr>
<td>Wire</td>
<td>2</td>
<td>120</td>
<td>1.65</td>
<td>0.45 - 0.85</td>
<td>0.10</td>
<td>0.01 - 0.02</td>
</tr>
<tr>
<td>Net (4L)</td>
<td>2 - 7</td>
<td>34 - 119</td>
<td>0.90 - 3.15</td>
<td>0.18 - 1.58</td>
<td>0.35 - 1.10</td>
<td>0.06 - 0.42</td>
</tr>
<tr>
<td>Total (4L)</td>
<td>154 - 239</td>
<td>2.55 - 4.80</td>
<td>0.63 - 2.43</td>
<td>0.45 - 1.20</td>
<td>0.07 - 0.44</td>
<td></td>
</tr>
</tbody>
</table>

Note: Net = Total Trace Length + Via + Solder Ball.

Cross Section

<table>
<thead>
<tr>
<th>Package Size (mm)</th>
<th>Ball Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 x 15</td>
<td>160, 176, 196</td>
</tr>
<tr>
<td>17 x 17</td>
<td>192, 196, 208, 217, 252, 256</td>
</tr>
<tr>
<td>17.2 x 17.2</td>
<td>512</td>
</tr>
<tr>
<td>19 x 19</td>
<td>272, 289, 292, 296, 297, 300, 301, 305, 324, 376</td>
</tr>
<tr>
<td>21 x 21</td>
<td>400, 456, 484</td>
</tr>
<tr>
<td>23 x 23</td>
<td>169, 192, 208, 217, 233, 241, 288, 301, 304, 305, 318, 320, 324, 338, 340, 348, 352, 360, 376, 386, 388, 420, 458, 480, 484, 492</td>
</tr>
<tr>
<td>27 x 27</td>
<td>225, 256, 272, 277, 292, 300, 312, 316, 320, 324, 336, 352, 384, 388, 400, 416, 456, 472, 480, 484, 496, 508, 512, 544, 580, 590, 636, 650, 676</td>
</tr>
<tr>
<td>35 x 35</td>
<td>04, 312, 313, 340, 352, 385, 388, 400, 420, 426, 432, 448, 452, 454, 456, 458, 474, 480, 484, 492, 516, 532, 542, 544, 548, 556, 564, 578, 580, 611, 624, 640, 648, 661, 665, 676, 680, 688, 700, 716, 729, 736, 740, 748, 756, 792, 816, 824, 840, 867, 886, 1012, 1156</td>
</tr>
<tr>
<td>37.5 x 37.5</td>
<td>435, 480, 552, 600, 601, 625, 627, 685, 701, 785, 788, 804, 840, 841</td>
</tr>
<tr>
<td>40 x 40</td>
<td>503, 557, 569, 596, 600, 745, 776, 928, 961, 1253</td>
</tr>
</tbody>
</table>

Package Configurations

2 die
3 die
(2 functional die + 1 spacer die)
4 die
(3 functional die + 1 spacer die)