VISION
公司愿景
Become First Ranking OSAT
建成全球数一数二的半导体封测企业

MISSION
公司使命
Provide Customer Satisfied OSAT Service with Best Value, and Maximize Payback to Employee, Shareholder and Society
提供客户满意的半导体封测服务，为客户创造最大价值，回馈员工、股东和社会

JCET
WORLD-CLASS SEMICONDUCTOR PACKAGING ASSEMBLY AND TEST COMPANY
世界级半导体封装测试企业

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Largest OSAT in China and the 3rd largest OSAT worldwide
Worldwide locations with six sites in Jiangyin, Chuzhou, Suqian, Singapore and Korea; and two major R&D centers in Singapore and mainland China
A global leader in semiconductor packaging & test technologies with extensive IP portfolio

- 中国大陆排名第一、全球第三
- 在江阴、滁州、宿迁、新加坡以及韩国拥有6处生产基地
- 主要研发中心在新加坡和中国大陆
- 封测技术及专利位列全球领导地位
1972
Jiangyin Transistor factory
Jiangyin Transistor Factory成立

1986
Discrete production
分立器件自动化生产线

1989
IC production
集成电路自动化生产线

1990
The workers' Congress in its inaugural speech
职工代表大会成立

1994
JV with Phillips
与飞利浦合作创办合资公司

2000
Restructured to company structure
公司改制

2003
ICAP offered WCSP
JCET IPO on Shanghai Stock Exchange

2005
Chairman of NAAT
国家集成电路产业技术创新联盟董事长

2007
D3 (IC) (SIP)
JCET IPO on Shanghai Stock Exchange

2009
MIS MIS封装材料厂成立

2010
Chairman of NAAT
刘家安

2011
D8 Suqian
长电科技（宿迁）公司成立

2012
D9 Chuzhou
长电科技（滁州）公司成立

2014
JV with SMIC
与中芯国际合资成立公司

2015
JCET acquired STATS ChipPAC
长电科技收购STATS ChipPAC

2016
The 3rd largest OSAT worldwide in 2016
跻身全球前三封测企业

2017
JCET Shanghai
长电科技上海分公司成立

1994
ST Assembly Test Services
STATS 建立封装测试服务

2004
STATS merges with ChipPAC
STATS与ChipPAC合并

2007
R&D Center established in Singapore
新加坡研发中心成立

2010
300-330mm eWLB MFG in Singapore
300-330mm eWLB技术

2013
Expansion of Singapore factory
新加坡工厂扩展

2017
SCC relocated to Jiangyin
昌信金品上海扩建至江门
Outsourced Semiconductor Assembly and Test Services (OSAT)

Full turnkey packaging and test solutions

Wafers from foundry

Drop Ship

Final Test

Assembly

Probe

Bump

RDL/TSV/IPD
滨江厂区
地址：滨江中路
占地面积：62,321平方米
建筑面积：58,300平方米
主要产品：凸块、晶圆级封装及测试

城东厂区
（含长电集成电路事业中心、长电先进、
新景、长电合肥）、
地址：长山路
占地面积：374,882平方米
建筑面积：372,500平方米
主要产品：晶圆级封装、凸块、倒装及
测试、插件级封装、基板封装、SIP

JCT D1, JCT-P-1, JCT-A, JSCC, SJK
地址：Changshu Road
Floor Area: 374,882 sqm
GFA: 372,500 sqm
Main Products: WL CSP, bumping, flip chip, Leaded, laminate, SIP, test, and MBS

宿迁厂区
地址：新金山路
占地面积：84,122平方米
建筑面积：53,700平方米
主要产品：大功率器件引线框架封装

JCT D8
地址：Purple Mountain Road
Floor Area: 84,122 sqm
GFA: 53,700 sqm
Main Products: Power package and test

滁州厂区
地址：世纪大道
占地面积：169,263平方米
建筑面积：85,000平方米
主要产品：小功率器件引线框架封装、
分立器件及测试

JCT D9
地址：Century Avenue
Floor Area: 169,263 sqm
GFA: 85,000 sqm
Main Products: Leaded, discrete package and test

韩国仁川厂区
地址：191 Jayumyeok-ro
Jung-gu, Incheon
占地面积：110,117平方米
建筑面积：110,200平方米
主要产品：SiP，芯片堆叠PoP，倒装及
测试

SCK, JSCK
地址：191 Jayumyeok-ro Jung-gu, Incheon
Floor Area: 110,117 sqm
GFA: 110,200 sqm
Main Products: SiP, flip chip, BGA, CSR, stacked
die, probe, assembly and final test

新加坡厂区
地址：5 Yishun Street
占地面积：29,894平方米
建筑面积：73,600平方米
主要产品：晶圆级封装、eWLB、测试

SCS
地址：5 Yishun Street
Floor Area: 29,894 sqm
GFA: 73,600 sqm
Main Products: Advanced wafer level packaging, laminate, QFN & test
**WAFFER LEVEL PACKAGE**

**Fan-in (FIWLP)**
- WLSCP
  - (Bumping, Repassivation, RDL)
- eWLSCP
  - (encapsulated WLSCP)

**Fan-out (FOWLP)**
- eWLBP
  - (embedded wafer level BGA)
- 2.5D and 3D SiP eWLBP

**Integrated Passive Devices**
- IPD

**Through Silicon Via**
- TSV for CIS
- TSV for 3D IC

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**Highlights**
- Compact, high performance packages for rapidly shrinking product form factors
- Proven leadership in innovative FOWLP solutions with over 1.7 Billion units shipped
- Innovative 2D/2.5D/3D FOWLP packages with size, performance and cost advantages
- Enhanced performance and size reduction with silicon IPDs
- 3D TSV capabilities covering mid-end-of-line through backend assembly and test

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**Technology Advantages**
- China's wafer-level packaging technology is the leader in FOWLP technology
- WLSCP products have exceeded 360 billion
- FOWLP products have exceeded 17 billion
- Integration of passive components on wafer level, more compact, small size, high performance
- As a leader in TSV technology, with complete 3D TSV packaging technology development and production capacity
**SYSTEM IN PACKAGE**

- FOWLP SiP
- Laminate FC SiP
- Laminate FC + WB SiP
- SiP Modules
- Leadframe WB SiP
- Laminate Stack Die WB SiP

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**Highlights**

- Electronic system or sub-system integrates multiple active and passive components for higher performance, functionality, processing speeds and low cost
- Leading SIP technology portfolio incorporates all the key technical building blocks
  
  -- Advanced design rules for 2.5D and 3D FOWLP or SiP configurations
  -- High density SMT with high accuracy component placement
  -- Advanced mold tech for complex topography SIP applications
  -- Highly automated process modules
  -- Tight process control to ensure consistency and high yield
- One stop turnkey solution - wafer to fully tested SIP modules

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**Advantages**

- SIP modules' packaging volume and quality rank among the top 3 globally
- Excellent technical service
- Advanced technology for high-speed and high-density SMT placement
- Customizable mold technology for complex SIP applications
- Highly automated processes ensure high yield and consistency
- One-stop solution from wafer to fully tested SIP modules

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- Target market: Various applications
- Customer benefit: Higher performance, functionality, processing speeds, and cost efficiency
**Flip Chip Package**

- **fcCuBE**
- **fcFBGA (fcCSP)**
- **fcBGA (FCBGA)**
- **Bare die fcPoP**
  - (flip chip package-on-package)

- **Molded Laser fcPoP**
  - (flip chip package-on-package)
  - (flip chip on Leadframe)
  - (FCOL)
  - **fcMIS**
  - (flip chip on Molded interconnect System)

**Highlights**
- Patented fcCuBE: proven low cost, high performance advanced flip chip technology
- Fine pitch Cu pillar and Bond-on-lead (BOL) interconnection for higher routing density at a lower cost
- Scalability to finer bump pitches, higher I/O, and advanced fab nodes at a lower cost
- High speed fcBGA-H offering for network/communication market
- fcPoP and hybrid flip chip + wirebond configurations for increased functional integration in a smaller form factor, and pre-stacking of memory on logic for PoP packages
- Leadership in low cost substrate technologies - Embedded Trace Substrate (ETS), Molded Interconnect System (MIS) and Single Layer laminate substrate

**Advantages**
- fcCuBE作为独特的倒装芯片封装专利技术，在提升性能的同时，有效地降低了封装成本
- 针对高速网络、高性能计算和消费类芯片市场，我们提供完整的fcBGA封装解决方案
- 进PoP封装技术可有效缩短内存芯片和逻辑芯片之间的互联，提高运算速度并降低功耗
- 基于引线框架MIS和铜凸块的FCOL专利倒装封装技术提供优异的导热导电性能
Highlights
- Advanced wirebond technology in a cost competitive manufacturing location
- Comprehensive range of single die, multi die, thermally enhanced and stacked die packages
- Thin outline LGA suitable for high performance and/or portable applications
- Low profile PoP provides flexibility in mixing and matching IC technologies in a thin package
- Innovative process capabilities to enable MEMS and sensors chipset integration and fusion
- Cost effective package approach for memory card formats

Wire Bond Package

Technical Advantages
- High yield and ultra-low defect rate
- Robustness against thermal and mechanical shocks
- Enhanced electrical performance
- Miniaturized design for space-saving solutions
- Compatibility with various industrial standards
- Improved reliability and longevity

Applications
- Memory cards
- Microcontrollers
- Memory modules
- Application-specific integrated circuits (ASICs)
- RF components
**Highlights**

- Extensive experience in leadframe and discrete packages for a wide range of applications
- Patented FCOL on MIS lead frame offers leading-edge QFN package for proven better electrical and thermal performance, particularly in power management applications

**Technology Advantages**

- Provides various applications of QFN packages
- QFNs offer multiple pin footprints for better I/O interconnect
- Leadframe technology provides superior performance
Patented molded interconnection technology that achieves higher density and performance for a wide range of packages with superior reliability.

**MIS advantages**
- Ultra small, thin technology achieves product miniaturization
- Superior RF, electrical, thermal and reliability performance
- Fine line routing for high density I/O
- Supports a wide range of wirebond, flip chip, SiP and PoP package configurations
- Proven substrate technology with over 1B units shipped since 2010

**MIS的优点**
- 超小、超薄的加工工艺使得产品更加微型化
- 优异的射频、导电性、导热性及可靠性
- 通过精细布线，实现更高的I/O引脚数
- 可应用于倒装、系统级封装等各类封装形式
- 自2010年以来，基于MIS基板技术的封装产品出货量已超过10亿颗
As one of the largest test outsourcing providers, we offer a full suite of test platforms and engineering services to support a broad range of mixed signal, RF, analog and high-performance digital semiconductor devices for the communications, digital consumer and computing markets. We combine operational efficiencies with proven test capabilities to achieve the lowest cost of test with the highest possible throughput and faster time-to-market.

**Full Turkey Services from Bump, Wafer Probe, Assembly, Final Test, Post Test To Drop Shipment**

- Bump
- Wafer Probe
- Assembly
- Final Test
- Post Test
- Drop Ship

**Test Engineering Services**

- Test program development, debug, optimization and validation
- Device characterization
- First silicon characterization (Wafer Probe)
- Load board design, fabrication and qualification (Final Test)
- Prototype evaluation
- Multi-site migration to higher parallel testing
- Test program conversion to new tester platform