XFBGA, XFLGA
Extremely Thin Profile Array Packages

Highlights
- Extremely thin packaging solutions
- Profile heights less than 0.50mm
- Advanced molding technology
- Extra thin design allows full array of solder balls (BGA) or lands (LGA)
- Available in single or multiple die solutions

Features
- Profile heights less than 0.50mm
- 0.25mm mold cap
- 50µm die thickness
- 0.11mm and 0.13mm substrate thickness (2 metal layer laminate substrate)
- Flexible body sizes ranging from 4 x 4mm to 15 x 15mm
- 0.80, 0.65, 0.50 and 0.40mm ball pitch
- 50µm solder bumping on substrate
- Utilizes conventional wirebond equipment and processes
- Wide range of custom and open tool designs available
- Pb-free material set options (including low alpha materials)
- JEDEC standard compliant

Description
Space constrained portable electronics such as cell phones, mini disk drives and miniaturized consumer electronics are driving the need for smaller and thinner packaging solutions to support low vertical profiles. By combining conventional wirebond equipment and processes with advanced thinning technologies, we are able to offer a leading edge solution that still satisfies the cost sensitive demands of consumer applications: Extremely Thin Profile Array Packaging solutions. Our extremely thin packages offer maximum profile heights less than 0.50mm.

While bare die solutions have typically been utilized for extremely thin profile requirements, we offer the option of using a substrate-based molded package for the same applications. These extra thin packages are able to accommodate die shrinks without changing the package footprint as well as integrate more than one device within the package.

In order to achieve a maximum profile height less than 0.50 mm, we utilize a 0.11mm and 0.13mm two metal layer laminate substrate, wafer thinning down to 50 microns, advanced molding technology and an optimized bill of materials to minimize warpage of the assembled package.

Our extra thin design allows a full array of solder balls or lands on the substrate to deliver greater flexibility in input/output (I/O), layout and density in a given package size. Our Extremely Thin Fine Ball Grid Array (XFBGA) package features a maximum height of 0.50mm while the Extremely Fine Land Grid Array (X1FLGA) package achieves a maximum height of 0.45mm.

We combine state of the art processing and equipment with proven material sets to achieve enhanced yield, reliability, and performance. Lead-free material sets are available for all extremely thin package types.

Applications
- Space constrained portable electronics such as cell phones, mini disk drives and miniaturized consumer electronics
- Memory cards and USB drives
- Stacked packages
Specifications

- **Die Thickness**: 50-100µm (2-4mils)
- **Mold Cap Thickness**: 0.25-0.30mm
- **Marking**: Laser
- **Packing Options**: JEDEC tray/tape & reel

Reliability

- **Moisture Sensitivity Level**: JEDEC Level 2A, 260°C Reflow
- **Temperature Cycling**: Condition C (-65°C to 150°C), 1000 cycles
- **High Temperature Storage**: 150°C, 1000 hrs
- **Pressure Cooker Test**: 121°C, 100% RH/2 atm, 168 hrs
- **Temperature/Humidity Test**: 85°C/85% RH, 1000 hrs
- **Unbiased HAST**: 130°C/85% RH/2 atm, 96 hrs

**Thermal Performance θja (°C/W)**

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, solder ball and land configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

<table>
<thead>
<tr>
<th>Package</th>
<th>Body Size (mm)</th>
<th>Pin Count</th>
<th>Die Size (mm)</th>
<th>Thermal Performance θja (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XFBGA</td>
<td>11 x 11 (2L)</td>
<td>144</td>
<td>4.5 x 4.5</td>
<td>46.48</td>
</tr>
</tbody>
</table>

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

**Electrical Performance**

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

<table>
<thead>
<tr>
<th>Conductor Component</th>
<th>Length (mm)</th>
<th>Resistance (mOmhs)</th>
<th>Inductance (nH)</th>
<th>Inductance Mutual (nH)</th>
<th>Capacitance (pF)</th>
<th>Capacitance Mutual (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire</td>
<td>2</td>
<td>120</td>
<td>1.65</td>
<td>0.45 - 0.85</td>
<td>0.10</td>
<td>0.01 - 0.02</td>
</tr>
<tr>
<td>Net (2L)</td>
<td>2 - 7</td>
<td>25 - 110</td>
<td>1.10 - 4.35</td>
<td>0.26 - 2.27</td>
<td>0.20 - 0.90</td>
<td>0.05 - 0.41</td>
</tr>
<tr>
<td>Total (2L)</td>
<td>4 - 0</td>
<td>145 - 230</td>
<td>2.75 - 6.00</td>
<td>0.70 - 3.12</td>
<td>0.30 - 1.00</td>
<td>0.06 - 0.43</td>
</tr>
</tbody>
</table>

Note: Results are simulated values per JEDEC EIA/JEP123 standards.

**Cross Sections**

- **XFBGA**
- **XFLGA**

**Package Configurations**

- **Body Sizes (mm)**: 4 x 4 to 15 x 15
- **Terminal Count**: 8 to 200+
- **Terminal Pitch (mm)**: 0.40 to 0.80
- **Typical Package Thickness**
  - XFBGA: 0.50mm max.
  - XFLGA: 0.50mm max.
  - X1FLGA: 0.45mm max.