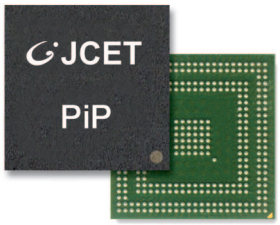
PiP

Package-in-Package: L/TFBGA-PiPs-SDx+y, LFBGA-PiPm-SDx+y

Highlights

- Stacking fully tested memory and logic packages eliminates KGD issues
- Provides the flexibility of combining a variety of structures to meet different functional needs in one package
- Package and board level reliability and board assembly same as conventional CSP



Features

- Package/die stack: 2 - 6 die stack
- 10 x 10mm to 23 x 23mm body size
- CSP package height at 1.2mm & 1.4mm max
- 0.4mm to 0.8mm ball pitch
- PIP body size can equal Internal Stacking Module (ISM) LGA size + 2mm
- Tested memory + logic/analog/RF combinations
- Allows flexible integration of tested memory & devices in small CSP package
- JEDEC standard package outlines (for ISM and FBGA)
- Thin die capability down to 40µm
- Thin mold cap down to 200µm for ISM LGA
- Low loop wire bonding, <50µm

Applications

- Integration of tested and burned-in memory with Baseband/ ASIC/Graphics processor in small form factors
- Competitive memory sourcing (packaged & tested)
- Allows for flexible mixed technology integration
- Portable electronics (Cellular phones, Gaming, PDAs, Digital Cameras, Camcorders, Wireless products
- 3D System in Package (SiP)

Test Services

- Product Engineering support
- Probe capability
- Program generation/conversion
- Drop ship available

Description

Package-in-Package (PiP) is an innovative family of 3D packages that stack packaged chips and bare chips into one JEDEC standard FBGA. A pre-tested Internal Stacking Module (ISM) Land Grid Array (LGA) and a BGA or a Known/Probed Good Die (KGD) are stacked and interconnected with wire bonding, then molded into a CSP that is indistinguishable from a conventional FBGA package.

A typical PiP integrates ASIC logic with memory chip(s), can have a minimal 12x12mm footprint, 1.2 to 1.4mm maximum thickness, and incorporate a 0.5mm to 0.4mm ball pitch. The PiP package can be assembled and board mounted like a conventional FBGA package and has equivalent package and board level reliability.

Advantages

3D packaging is driven by wireless and consumer products that need package level functional integration in the smallest footprint, lowest profile and lowest cost CSP. Stacked die for Flash, SRAM and DRAM memories in a CSP are widely available today from memory suppliers but require KGD (especially for DRAM). As integration is extended to include complex and costly chips like ASIC in the same package with more Memory and Analog or RF chips, stacked packaging solutions are increasingly being utilized to maximize final test yield, expand supply chain and minimize the cost of ownership.

PiP enables new functionality in the shortest time-to-market and with minimum risk by stacking tested packages and known good logic or analog die sourced from the established supply chain. A lower PiP packaging cost, compared to the equivalent cost of separately packaged chips, and significantly reduced final test complexity both result in a module with lower cost of ownership.

Standard Materials

Wire	18 - 25µm (0.7 - 1.0mil) diameter
Mold Compound	Epoxy resin
Solder Ball	SnPb or SAC (Pb-free)
Packing Options	JEDEC tray or tape & reel

Process Highlights

Stacking	2-6 die in various configurations: 1-2 die on base substrate (bare or in BGA) + 1-4 die in ISM LGA (tested package)
Wafer Thinning	Down to 40µm thick on 200/300mm wafer
Wire Bonding	ISM LGA can have up to 2mm overhang
Molding	Down to 0.20mm mold cap for ISM LGA
Marking	Laser

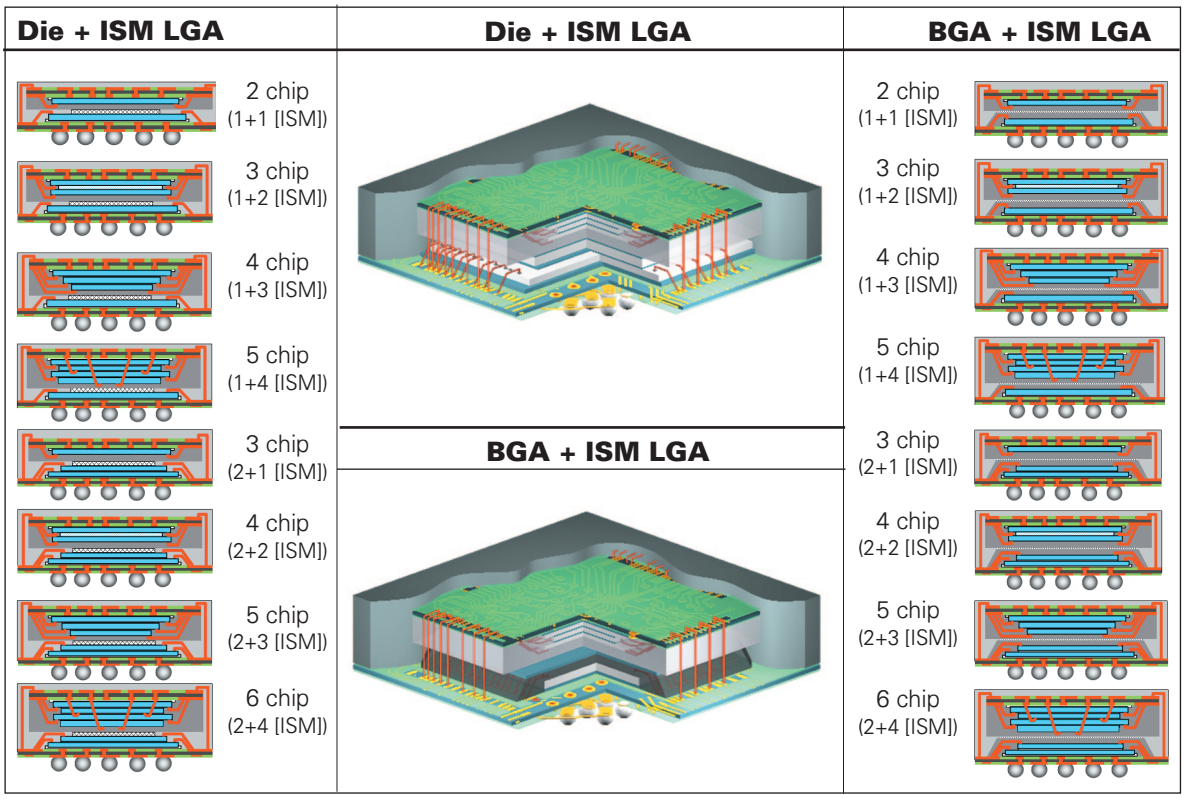
Reliability (Preconditioning Level @ 260°C 3xIR reflow)

Moisture Sensitivity Level	JEDEC Level 2A (60°C/60%, 120 hrs)
Temperature Cycling	Condition C w/precon, 1000 cycles
Temperature/Humidty Test	85°C/85%, RH, 1000 hrs
Highly Accellerated Stress Test	135°C/85% RH, 2 atm, 96 hrs
High Temperature Storage	150°C, 1000 hrs
Thermal Cycle	Condition C, -65°C/150°C, 1000 cycles

Package Configurations

Typical Body Sizes	10x10, 12x12, 13x13, 15x15, 17x17mm, 21x21mm, 23x23mm
Ball Count	40 to 450
Ball Pitch	0.4 to 0.8mm
Package Thickness	Up to 3 chips: 1.2 thick Up to 4 chips: 1.4 thick Up to 6 chips: 1.6 thick

Cross Sections



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