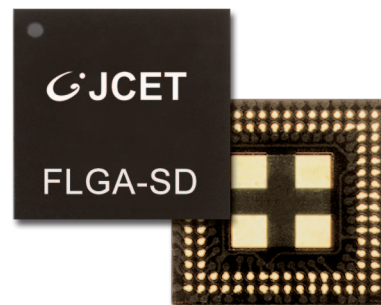


FLGA-SD

Fine Pitch Land Grid Array - Stacked Die

Highlights

- Stacking of die allows for more functionality in an array molded, cost effective, space saving package solution
- Available in a variety of package heights including 2.45mm (LFLGA-SD), 1.2mm (TFLGA-SD), 1.0mm (VFLGA-SD), 0.8mm (WFLGA-SD), 0.65mm (UFLGA-SD) and 0.5mm (XFLGA-SD) maximum thickness
- Thinner than FBGA
- Exposed thermal/mechanical lands available
- Back side SMT
- 2 to 6 layer laminate substrate



Features

- 2 to 8 die stack with spacer capability
- Flexible body sizes range from 4 x 4mm to 12 x 18mm
- 0.5, 0.65, 0.80, 1.0, 1.2, 1.4, 2.45mm max package height
- Flexible die stacking options (pyramid, same die, etc.)
- 0.5mm minimum land pitch, flexible land pattern
- Memory, Logic, Analog and RF combinations
- JEDEC standard package outlines
- Die thinning to 40μm (1.6mils) capability
- Low loop wire bonding; reverse and die to die
- Up to 2mm die overhang per side
- Halogen-free and Low-K wafer compatible BOM
- Film spacer capability for decreased die stack thickness
- Very thin substrate capability
- Capability to integrate discrete passives or integrated passive devices (IPD)
- Film spacer capability for decreased die stack thickness
- Solder bump capability
- Test capability

Description

Our chip stack technology offers the flexibility of stacking 2 to 8 die in a single package. Die to die bonding capability enables device and signal integration to improve electrical performance and reduce overall package I/O requirements. Wafer thinning technology, overhang wire bond technology, and the use of spacers between stacked die provide the flexibility to stack almost any desirable configuration of die in one package. This capability uses existing assembly infrastructure, which results in more functional integration with lower overall package cost.

The use of the latest packaging materials allows this package to meet JEDEC Moisture Resistance Test Level 2a with Lead-free reflow condition. This is an ideal package for cell phone applications where Digital, Flash, SRAM, PSRAM and Logic are stacked into a single package.

Applications

- Handheld devices
- Wireless RF
- Analog
- ASIC
- Memory
- Simple PLDs



Specifications

Die Thickness	50-300 μ m (3-12mils)
Gold Wire	15-30 μ m (0.6/0.8/0.9/1.0/1.2mils) diameter
Pd/Cu Wire	15-25 μ m (0.6/0.7/0.8/1.0mils) diameter
Ag Wire	18-25 μ m (0.7/0.8/1.0mils) diameter
Mold Cap Thickness	0.25-1.22mm
Marking	Laser
Packing Options	JEDEC tray/tape & reel

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (-65°C to 150°C), 1000 cycles
High Temperature Storage	150°C, 1000 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

Electrical Performance

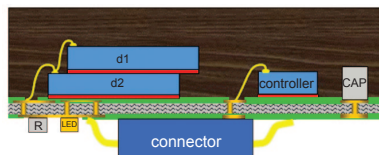
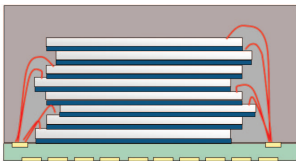
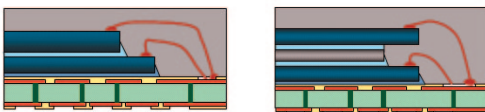
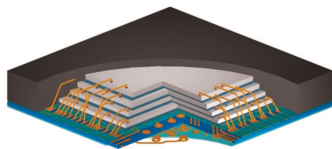
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	25 - 110	1.10 - 4.35	0.25 - 2.27	0.20 - 0.90	0.05 - 0.41
Total (2L)	4 - 0	145 - 230	2.75 - 6.00	0.70 - 3.12	0.30 - 1.00	0.06 - 0.43
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	25 - 110	0.70 - 2.95	0.17 - 1.57	0.30 - 1.05	0.05 - 0.41
Total (4L)	4 - 9	145 - 230	2.35 - 4.60	0.62 - 2.42	0.40 - 1.15	0.06 - 0.43

Note: Net = Total Trace Length + Via

Cross Sections

FLGA-SD



Package Configurations

Body Sizes	4x4 to 12x18mm
Terminal Count	8 to 200
Terminal Pitch	0.5 to 0.8mm
Typical Package Thickness	LFLGA-SD: 2.45mm max. TFLGA-SD: 1.2mm VFLGA-SD: 1.0mm max. WFLGA-SD: 0.8mm max. UFLGA-SD: 0.65mm max. XFLGA-SD: 0.5mm max.

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