

**“FlexLine™ - A Universal Wafer-Level Packaging  
Platform for Fan-In and Fan-Out Designs”**

by

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# FLEXLINE™ - A UNIVERSAL WAFER-LEVEL PACKAGING PLATFORM FOR FAN-IN AND FAN-OUT DESIGNS

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## ABSTRACT

A new flexible manufacturing methodology has been developed that provides a seamless bridge between the manufacture of fan-in and fan-out wafer level package designs while retaining the same fundamental process flow and materials. The fan-out packages produced (trade named eWLB for embedded wafer level ball grid array) provide a superior alternative to traditional leadframe- and substrate-based packaging and have received broad industry adoption. The fan-in configuration produced with this methodology, known as eWLCSP™ for encapsulated Wafer Level Chip Scale Package, is relatively new and unique in the industry, providing a superior alternative and drop-in replacement for the traditional WLCSP package.

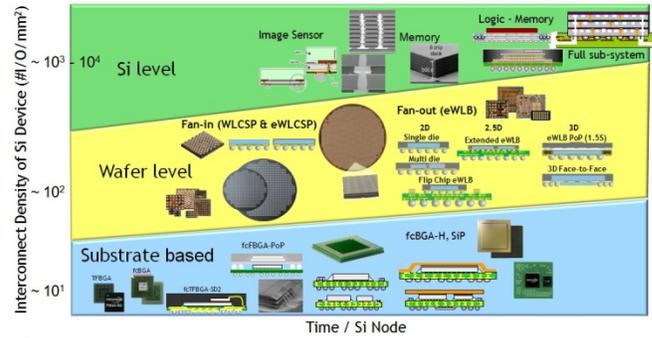
In this paper, we review the new flexible manufacturing methodology, the attributes of the resulting fan-out and fan-in package architectures, and more notably, the features of the new fan-in package known as encapsulated WLCSP or eWLCSP™. We also present the exceptional scaling of density, form factor and cost that is made possible by this packaging approach. Finally, we review the future avenues for further expanding the scale and cost of the manufacturing process.

Key words: eWLB, fan-out, eWLCSP, fan-in, wafer level package, reconstitution, FlexLine.

## INTRODUCTION

Packaging technology has seen many significant shifts over the past few decades in step with increases in the I/O density of the silicon (Si) device being packaged. This includes transitions from leaded packaging to laminate packaging and subsequently from plated through-hole laminate substrates to build-up substrates. These transitions have in turn enabled denser forms of interconnection such as the transition from wire bond to flip chip.

An analysis of the recent changes in I/O density heralded by the rapid transitions in Si nodes shows that we are likely on the cusp of yet another such shift in packaging technology, as shown in Figure 1. With I/O densities quickly exceeding the traditional 10-20 I/O per mm<sup>2</sup> range, a wafer level packaging approach which is based on thin film processing presents a logical platform solution to the density demands posed by upcoming Si devices [1].



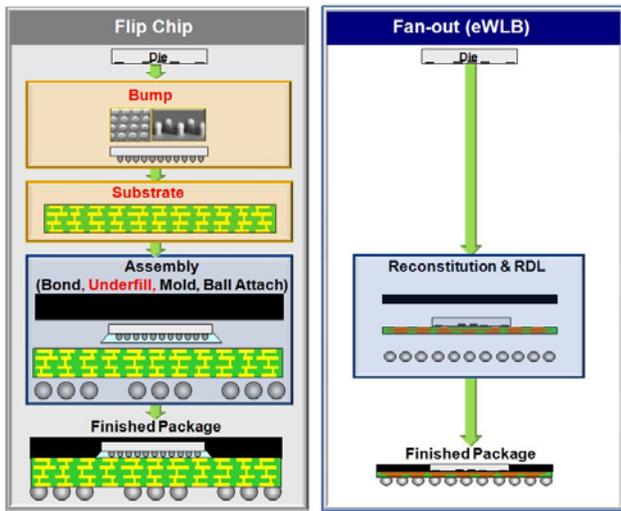
**Figure 1:** I/O density trend in Si and the evolution of packaging technology

To further explain this point, the density and form factor scaling associated with a wafer level packaging approach is illustrated by way of a comparison between a traditional flip chip and a fan-in/fan-out wafer level package architecture in Table 1. The 1.5 – 2x scaling achieved is commensurate with what is needed to meet the I/O density demand of Si devices as previously mentioned.

**Table 1:** Density scaling with fan-out wafer-level packaging

Package Platform	Feature Density		Feature Thickness	
	L/S (um) (X-Y)	Via Pitch (um) (Z)	Dielectric Thickness (um)	Conductor thickness (um)
Flip Chip	20/20	100	25/ 50 um (Build-up/Lam)	10/30 um (additive/subtractive)
Fan-out/eWLB	10/10	50	5 - 10 um (customizable)	4-8 um (customizable)

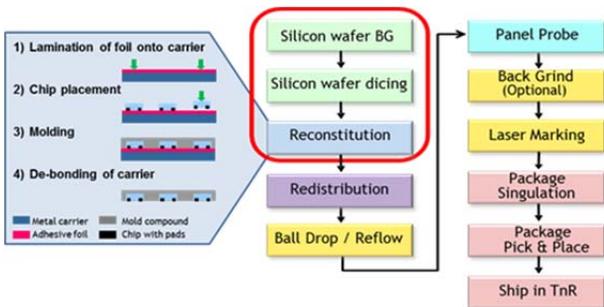
Notably, the transition to fan-in/fan-out packaging also entails significant paradigm shifts in the manufacturing approach and basic process flows, as depicted in Figure 2 wherein, a comparison with traditional flip chip packaging is used for illustration. Firstly, whereas traditional leaded and laminate packaging entails the independent production of a die and a substrate and the process of bonding them together, in fan-out/fan-in wafer level packaging, the “substrate” is essentially “built on the die” through thin film processing. Secondly, and referring more specifically to the incumbent flip chip packaging approach, the traditional bump and substrate are completely obviated, the former being replaced by a direct thin film interconnection to the bonding pad on the die and the latter by the thin film circuitry itself, comprising dielectric and conductor layers.



**Figure 2:** Comparison of flip chip and wafer-level fan-out (eWLB) processes

### FAN-IN/FAN-OUT PACKAGING PROCESS – ONE SIZE FITS ALL!

A new methodology known as FlexLine™ has been introduced as an innovative approach to wafer level manufacturing that encompasses both fan-in and fan-out packages on a single line. A schematic of the Flexline manufacturing process is illustrated in Figure 3. FlexLine is based on a well-established, high volume manufacturing process for fan-out eWLB packages. While there are multiple variants of fan-out manufacturing in development in the industry today, the FlexLine manufacturing flow depicted in Figure 3 represents the unique process and architecture as engineered by STATS ChipPAC and successfully implemented in the volume production of eWLB several years ago [2,3].



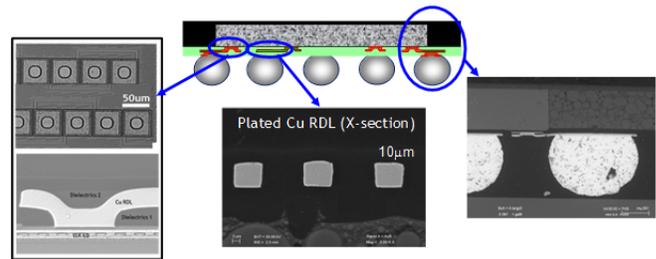
**Figure 3:** FlexLine process flow for fan-in/fan-out wafer level packaging

As is evident from Figure 3, the process steps are similar to the more familiar WLCSP manufacturing process [4] with the exception of *reconstitution* which is unique to eWLB and the FlexLine process. To provide a better understanding of reconstitution, the process flow is further broken down into its four sub-steps comprising (i) application of an adhesive layer to a carrier; (ii) accurate face down placement of the die on to the carrier; (iii) encapsulation of the die using a proprietary compression molding process; and (iv) removal of the carrier, resulting in a self-standing

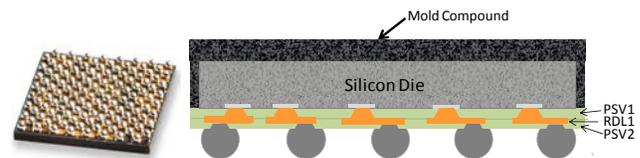
*reconstituted wafer* with the active surfaces of the die exposed.

An important distinction with the FlexLine process is that the reconstituted wafer does not require a carrier for subsequent processing and handling. Also, as alluded to earlier, there is no bumping step in this process as the contact between the package circuitry and the die pad is formed directly through the thin film deposition process. The implementation of this process in a 300 mm carrier format has been described in previous work [3].

The basic structure of an eWLB package produced by the above process is illustrated in Figure 4. While the configuration shown in Figure 4 is a fan-out design, it is important to understand that a fan-in configuration can be seamlessly implemented using the exact same process by merely performing the final singulation very close to the edge of the die with no terminal solder balls beyond the shadow of the die. Such a fan-in configuration is depicted in Figure 5 and described in detail in the next section. It is evident in Figure 5 that the die effectively becomes encased in a layer of polymer on its four side walls as well as on its back side as a natural attribute of the basic fabrication process. Hence, we have aptly named this fan-in package configuration eWLCSP for encapsulated wafer level CSP.

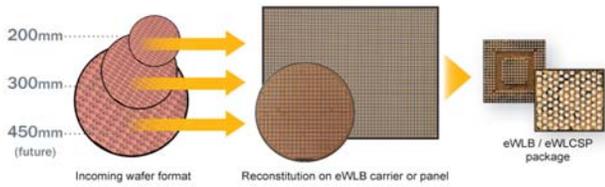


**Figure 4:** Basic structure of eWLB package



**Figure 5:** eWLCSP Package Structure

Another unique and highly beneficial feature of the FlexLine packaging process is the ability to seamlessly service any incoming Si wafer diameter without a change to the manufacturing process or bill of materials. By normalizing incoming wafer diameters to a uniform processing size, the process is essentially wafer agnostic and does not require a change based on the diameter of the incoming or parent wafer. This point is illustrated more clearly in Figure 6. Thus, not only is the process seamless with regards to fan-in vs. fan-out designs, but it is also seamless in its ability to handle multiple wafer diameters.

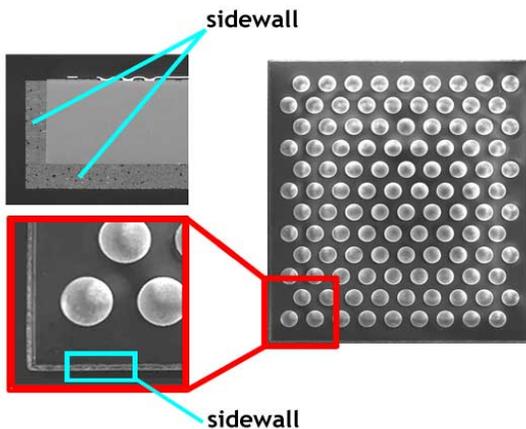


**Figure 6:** Illustration of FlexLine wafer-agnostic approach

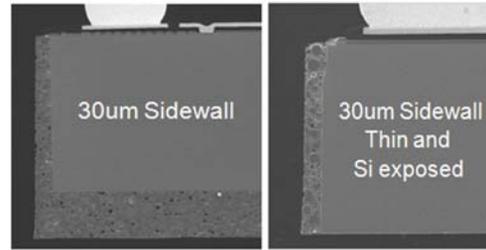
This has two important practical implications. First, separate investments that are normally required to service different parent wafer diameters (particularly with transitions from 200 mm to 300 mm and to 450 mm in future) are obviated as one common carrier technology can handle any parent wafer. Second, the pooling of capacity across all the eWLB, eWLCSP and other eWLB-derivative package configurations as well as across different wafer formats results in a single streamlined process flow and considerable economies of scale and resultant reduction in manufacturing cost.

**eWLCSP™: THE UBIQUITOUS WLCSP MORPHS INTO SOMETHING BETTER!**

As a bare die package with exposed Si surfaces, traditional WLCSPs are often exposed to mechanical damage such as chipping and cracking in the course of processing, shipping and during surface mount technology (SMT) operations. This is particularly true for advanced Si node products where the die is very thin and dielectric layers are extremely fragile. With the FlexLine process, fan-in eWLCSPs have the same encapsulation advantages as fan-out eWLB. The typical structure of eWLCSP is shown in Figure 7 with micrographs of the cross section view in Figure 8. The eWLCSP is functionally equivalent to a traditional WLCSP with the addition of a sidewall and an optional backside layer of polymer material [5]. While the structure shown in Figure 7 is typical, many variants of the base structure have been demonstrated. For example, the backside molding compound can be removed with an optional back grind operation and the body made thinner while still retaining the protective sidewall layer as in Figure 8.

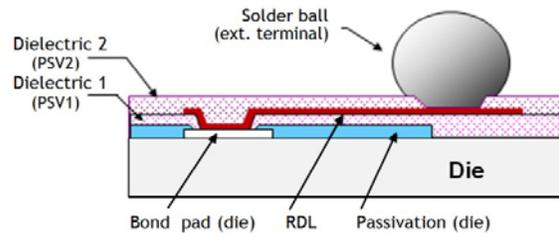


**Figure 7:** Example of eWLCSP sidewall



**Figure 8:** X-section view of eWLCSP – standard overmolded version and thin version with exposed Si back side

While there is considerable latitude in the choice of the number of metal and dielectric layers and thicknesses in eWLCSP, a “1L RDL structure” as shown in Figure 9 is the most typical. Note that in the typical case, no under bump metal (UBM) layer is necessary; the terminal solder balls are attached directly to the RDL metal layer through a suitably designed dielectric (PSV2) opening. This unique feature, which essentially amounts to the elimination of one lithography step, is made possible with the use of carefully engineered dielectric materials and design geometries. This has been proven out through extensive board level reliability (BLR) testing with very high volumes of product shipped for various mobile applications.



PSV 1 (um)	7.0 - 11.0
RDL (um)	7.0 - 10.0
PSV 2 (um)	7.0 - 11.0
Ball pitch (mm)	0.4
S'ball size (um)	250

**Figure 9:** eWLCSP 1 layer RDL configuration

**ADVANTAGES OF eWLCSP: THERE IS SUCH A THING AS A FREE LUNCH!**

The structure and manufacturing process for eWLCSP bring a number of unique and compelling advantages which address the primary areas of concern associated with the traditional WLCSP solution [5] as referred to earlier.

**(1) Cost! Cost! Cost!**

As described above, eWLCSP is fabricated using reconstitution. Good die from the parent wafer are picked and transferred to a (larger) reconstituted carrier. Since the majority of WLCSP products use 200 mm wafers, reconstitution enables the scaling of the manufacturing process from the 200 mm wafer to the size of the carrier used in volume production of eWLB technology. This carrier size ranges from 200/300 mm to a larger format like high density (HD) with > 20% more area or Ultra High

Density (UHD) with > 200% more area. The HD format is currently in mass production. The scaling of the manufacturing process with reconstitution far outweighs the cost of reconstitution itself; thereby enabling large net cost reductions for devices produced on 200 mm wafers.

Additionally, the ability to selectively pick good die from the parent wafer presents an additional net cost benefit as most wafers have a < 100% wafer sort yield. Last but not least, the ability to pool the manufacturing volume of traditional fan-out eWLB packages seamlessly together with eWLCSP packages on the same FlexLine™ provides important economies of scale.

**(2) Quality! Quality! Quality!**

The polymer sidewall structure of eWLCSP all but eliminates mechanical damage such as chipping and cracking that is commonly encountered in traditional WLCSP processing. This serves to eliminate many expensive steps such as back side coating or lamination and complex inspection steps that are currently necessary for standard WLCSP to manage mechanical damage and ensure product quality. More fundamentally, eWLCSP allows customers to *build in quality by design* vs. using inspection to weed out defects. This has implications for reducing the risk of field failures due to the shipment of marginally defective parts that may escape inspection. As shown in a later section, the encapsulated eWLCSP structure has also helped to increase the overall die strength by ~ 50% in addition to the mitigation of cracking and chipping defects, making for an overall more robust package.

**(3) Investment/Infrastructure – Wafer Agnostic Processing**

In traditional WLCSP processing, the investment and infrastructure for manufacturing are based on the diameter of the incoming wafer. This creates a financial burden to re-tool the manufacturing lines to provide the needed capacity (to meet market demand) as wafer transitions occur (e.g. from 200 mm to 300 mm or from 300 mm to 450 mm in future) while also having to obsolete the existing manufacturing assets. The FlexLine approach for eWLB and eWLCSP effectively decouples the packaging process from the incoming wafer altogether, obviating the above-described financial burden resulting from wafer diameter transitions (illustrated in Figure 6).

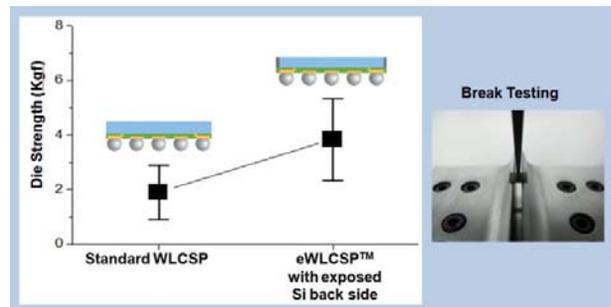
**(4) Design – Seamless transition from Fan-in to Fan-out**

The standard fan-in WLCSP only works below a certain threshold of I/O density, based on the minimum allowable terminal I/O pitch. The threshold is ~ 4 I/O /mm<sup>2</sup> for a 0.5 mm terminal I/O pitch and ~ 6 I/O /mm<sup>2</sup> for 0.4 mm terminal I/O pitch. Small changes in I/O density that commonly occur with changes in Si design or die shrinks resulting from Si node transitions may lead to a given design exceeding the WLCSP threshold, causing the design to “fall off” the WLCSP application space envelope, [1] necessitating a change in the packaging plan of record (POR) to traditional substrate- or leadframe-based packages

like FBGA, fcBGA, QFN, etc. These packages are fundamentally different than WLCSP in terms of footprint, form factor, performance and cost, resulting in a major “reset” in the packaging POR. In contrast, eWLCSP may be viewed as part of the more universal eWLB platform wherein the aforementioned I/O density transitions can be seamlessly accommodated within the same packaging platform. For designs whose I/O density falls marginally outside the threshold, an additional row of terminal solder balls can be added without fundamentally altering the package structure, form factor or performance.

**eWLCSP RELIABILITY – QUALITY DESIGNED IN**

The protective polymer sidewall feature not only helps prevent Si chipping and cracking, but also provides protection against mechanical breakage during socket insertion for electrical testing. While multi-site probe testing at the reconstituted wafer level is common for many applications, eWLCSP enables the prospect of conventional socket testing, often a more simple and cost effective alternative especially for larger die sizes. The viability of socket testing without mechanical damage to the part has been demonstrated through multiple insertion tests. To quantify this effect, it was shown through break testing that the break strength of a typical eWLCSP package (4.7 x 4.7 mm body size with 30 um side wall and exposed Si structure) had comparable back side Si surface roughness, but approximately 2x the break strength (Figure 10).



**Figure 10:** Mechanical break strength comparison of eWLCSP and traditional WLCSP

The eWLCSP process has passed standard reliability tests used in wafer level packaging, which includes Component Level Reliability (CLR), Temperature Cycle on Board (TCoB), and Drop Test. CLR was completed on a 4.7 x 4.7 mm package with 1L RDL structure as illustrated in Figures 7-9, and using the test conditions as shown in Table 2. The response variables were electrical continuity, delamination, solder ball shear strength and visual/mechanical damage with measurements performed pre- and post- stressing.

**Table 2**

Component Level Test	Condition		Status
MSL1	MSL1, 260C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55°C to 125°C	1000 x	Pass
HAST (w/o bias) after Precon	130°C / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150°C	1000 hrs	Pass

BLR testing comprising TCoB and Drop Testing was also performed. TCoB passed 500 cycles to first failure and Drop Test passed the JEDEC requirement of 30 drops (Table 3).

**Table 3**

Tests	Conditions	Failure Rate	Characteristic life ( $\eta$ )	Weibull slope ( $\beta$ )	First Failure
TCoB (Cond B)	-40°C to 125°C	0.635	1219.4	10.13	864x
Drop Test	JEDEC	0.635	1553.5	5.97	772x

Preliminary predictive modeling has shown that the BLR reliability of eWLCSP should far exceed that of WLCSP in view of the mechanically balanced structure of the polymer encased configuration. Systematic comparative studies of BLR between eWLCSP and WLCSP packages using a combination of FEA (finite element analysis), empirical TCoB and drop testing are currently under way and will be a subject of a subsequent paper.

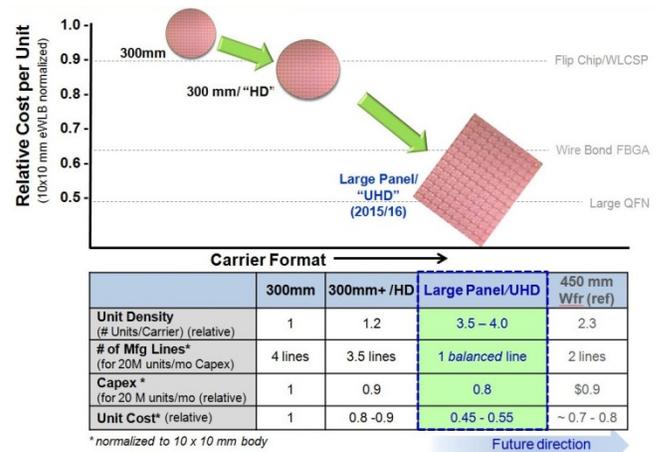
### FUTURE SCALING OF THE MANUFACTURING PROCESS – THE “GOLDILOCKS” SOLUTION

Two broad groups of manufacturing infrastructure are currently prevalent in the packaging industry. The PCB/IC substrate manufacturing infrastructure which handles large organic substrates in a rectangular format and uses plating/etching techniques for circuitization; and, the wafer fabrication (wafer fab) infrastructure which handles round wafers using thin film/PVD (physical vapor deposition) techniques for circuitization. While the former lends itself well for packaging applications in terms of cost, it lacks the scalability to higher density demanded by the trajectory of escalating Si device I/O density (as illustrated in Figure 1 earlier). On the other hand, the latter provides orders of magnitude higher density (sub-micron or nano-scale feature sizes), but remains largely an overkill for the needs of packaging applications. We view the eWLB manufacturing approach to be the “Goldilocks” solution, as it is just right for what is needed. It leverages the density benefits of thin film processing while retaining the lower cost structure of PCB/IC substrate manufacturing.

When production started several years ago, the wafer fab processing approach was adopted for reasons of expediency (ease of availability of manufacturing tools) while adding a number of cost-reducing process adjustments. In terms of the future, there is room for fundamentally optimizing the manufacturing infrastructure to achieve significantly better capital intensity and unit cost by finding approaches that can be tailored specifically for the eWLB process. As an example, larger carrier sizes can be used that sacrifice the capability for overly fine sub-micron or nano-scale design rules, but significantly improve capital intensity and cost.

Our studies have shown that a carrier format similar to the large panels used in large area display LCD manufacturing is a good candidate. Figure 11 depicts the estimated magnitude of scaling and associated productivity/cost improvements that are achievable by using this approach compared to a traditional wafer fab infrastructure.

Furthermore, the manufacturing tools can be tailored to be optimum for the specific requirements of the eWLB process. This becomes viable as the industry adoption of eWLB increases.



**Figure 11:** Next generation manufacturing infrastructure

We are at that watershed moment today. Increased adoption by the customer base has already ushered in a greater number of participating packaging companies into the mix, making the technology more prevalent and multi-sourcable. This has also triggered interest among the leading equipment manufacturers to participate in the associated equipment business. Development of this next generation manufacturing solution is currently under way.

### SUMMARY & CONCLUSIONS

There is a growing demand for wafer level packaging in advanced mobile products. Despite the successful adoption of fan-in wafer level packaging technology, there continued to be a number of concern areas, notably: (i) a capital investment structure that remains exposed to wafer size transitions, e.g. from 200 mm to 300 mm and to 450 mm in future; (ii) the risk of cracking, chipping and other forms of handling damage and the associated quality implications; and (iii) a “fan-in only” package architecture that dictates switching to fundamentally different packaging solutions when small changes are required in the I/O density of the device.

A novel manufacturing process and associated package platform for wafer level packaging is developed that addresses the aforementioned concerns while providing a more robust and lower cost solution across the entire fan-in/fan-out design space. Notably, the new fan-in configuration termed encapsulated WLCSP (eWLCSP™) is introduced which features a unique polymer sidewall structure and can be deployed as a seamless drop in replacement of standard WLCSP packages.

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