“Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as Innovative 2.5D Packaging Solutions”

by

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Abstract
The market for portable and mobile data devices connected to a virtual cloud access point is exploding and driving increased functional convergence as well as increased packaging complexity and sophistication. This is causing an unprecedented demand for a variety of wafer level packages, thin Package-on-Package (POP) and 3D System-in-Package (SiP) solutions. We expect to see more exciting interconnect technologies in wafer level packaging such as 3D Through Silicon Via (TSV), 2.5D interposers, eWLB (embedded Wafer Level Ball Grid Array) / FOWLP (Fan-out Wafer Level Packaging) and innovative 2.5D/3D eWLB technology to meet these needs.

eWLB is a fan-out wafer level packaging (FOWLP) technology that enables a higher ball count by extending the package size beyond the area of the chip. By utilizing eWLB’s fan-out packaging approach, the next level of multi-chip and thin packaging capability can be achieved. eWLB provides a robust packaging platform supporting very dense interconnection and routing of multiple die in very reliable, low-profile, low-warpage 2.5D and 3D solutions. The use of advanced eWLB designs such as a side-by-side configuration can replace a stacked package configuration or be utilized as the base for a 2.5D/3D TSV configuration in order to achieve a more cost effective packaging solution.

Combining an analog or memory device with a digital device can provide an optimum solution for achieving the best performance in situations where thin, multi-die and heterogeneous integration is required for very high performance applications.

This paper will highlight the rapid trend towards extended eWLB and flip chip eWLB in high performance packaging technology. A study will be presented on flip chip substrate design optimization in combination with eWLB RDL technology. Mechanical simulation was carried out to investigate the stress on bumps and device stack layers with different bumping approaches. Extended eWLB / flip chip eWLB offers a cost-effective solution for advanced node technology with a smaller pitch required for high performance applications. Extended eWLB and flip chip eWLB technology provide the benefit of integration as well as a lower cost solution without sacrificing electrical performance.

I. INTRODUCTION
Wafer level packaging (WLP) applications are expanding into new areas and are segmenting based on I/O count and type of device. The traditional design layout of passive, discrete, RF and memory device is expanding to logic ICs and MEMS. The WLP segment has matured over the past decade with numerous companies delivering high-volume applications across multiple
wafer diameters and expanding into various end-market products. With the WLP infrastructure and high volume production already in place, a major focus area now is cost reduction.

One of the most well known examples of a FOWLP structure is eWLB technology [1]. This technology uses a combination of front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer which can greatly reduce manufacturing costs. The benefits of eWLB include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count and maximum connection density as well as desirable electrical and thermal performance. eWLB also offers a high-performance, power-efficient solution for the wireless market [2]. Furthermore, 2.5D/3D eWLB technology enables 2.5D interposer packaging, 3D IC, and 3D SiP (System-in-Package) with vertical interconnection. 2.5D/3D eWLB can be implemented with heterogeneous integration of IPD, MLCC or discrete component embedding.

II. eWLB Technology

eWLB TECHNOLOGY

eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. On the other end there are physical constraints such as footprint and height. Other parameters that were considered during the development phase included I/O density which is a particular challenge for small chips with a high pin count, the need to accommodate SiP approaches, thermal issues related to power consumption and the device’s electrical performance (including electrical parasitic and operating frequency) [3].

eWLB is an interconnection system processed directly on the wafer and compatible with motherboard technology pitch requirements. It combines conventional front- and back-end manufacturing techniques with parallel processing of all chips.

Figure 1. (a) eWLB wafer after packaging with reconstitution, RDL and backend processes and (b) schematics of innovative eWLB structures.

There are three stages in the eWLB process; i) reconstitution, ii) RDL and iii) backend & test. Additional fab steps create an interconnection system on each die, with a footprint smaller than the die itself. Solder balls are then applied and parallel testing is performed on the wafer. Finally, wafers are sawn into individual units, which are used directly on the
motherboard without the need for interposers or underfill. Figure 1 shows an example of an eWLB wafer and package structures for 2D to 3D applications. A SEM photo of an eWLB package is shown in Figure 2.

**Figure 2.** SEM micrographs of cross-section of eWLB. (total package body thickness ~500um)

**Advantages of eWLB Technology**

Today BGA package technology is limited by the capability of the organic substrate. eWLB helps to overcome such limitations and also simplifies the supply chain. Building the substrate on the package itself allows for higher integration and routing density in less metal layers. eWLB is an innovative packaging platform that will support future integration, particularly for mobile and high performance devices and this packaging technology has a number of important features. Transition to eWLB packaging technology enables a significant reduction in recurring costs by eliminating the need for expensive substrates. The advantage of eWLB packaging can be summarized in Table 1. BGA packaging also faces a challenge with technology nodes beyond 28nm as the device performance density drives the need for flip chip interconnect. However, extreme low-k (ELK) dielectric structures used in conjunction with advanced Si nodes are more fragile and are therefore more susceptible to cracking or delamination during flip chip assembly, resulting in flip chip becoming narrower in terms of packaging process margin. In addition, there is a growing trend in environmentally friendly packaging with lead free, halogen free, or green material sets. With ELK and interconnect pitches becoming smaller and smaller and the shift to lead free materials, the technical limitations faced by the packaging industry are becoming more challenging. eWLB technology provides a window for packaging next generation devices in a generic, lead-free/halogen free and green packaging scheme.

<table>
<thead>
<tr>
<th>Advantage of eWLB Packaging</th>
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<tr>
<td>MCP configurations (down to 0.5mm)</td>
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<td>The thinnest 3D solution (stacked thickness down to 0.8mm)</td>
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<td>Scalable heterogeneous integration platform</td>
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<td>Leading cost/performance solutions (co-design optimized)</td>
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<tr>
<td>Ultra fine ball pitch and maximum I/O density</td>
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<tr>
<td>Excellent electrical and thermal performance</td>
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<td>Enhanced reliability with advanced dielectric materials</td>
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<td>PoP configurations - both single and double sided</td>
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**III. EXTENDED eWLB / FLIP CHIP eWLB[4]**

**Extended eWLB**

The use of eWLB packages in a side-by-side configuration to replace a stacked package configuration or to function as the base for a 2.5D TSV
interposer configuration is critical to enable a more cost effective packaging solution. Combining LSI with the wide I/O memory interfaces or high bandwidth memory (HBM) with the TSV packaging capability can provide an optimum solution for achieving the best performance in thin multi-die stacks for very high volume manufacturing. A comparison of a TSV interposer solution to an eWLB based solution is shown in Figure 3.

2.5D interposer technology offers several advantages including:

- IP block partition: De-coupling functional blocks in SoC (analogue, memory, I/O, RF)
- Heterogeneous package integration
- Lower power dissipation
- Lower total device cost

However, there are still many challenges to apply interposer technology to market applications. One of the key challenges is the supply of TSV interposers with cost effective solutions. Silicon wafers are one of the primary materials used and there are active research and development activities for glass, poly-Si or other materials.

eWLB has the capability of multi-die and multi-RDL structures as well as less than 10um/10um LW/LS capability. In addition, there have been advancements in eWLB integration with different components such as Si device, IPD, discrete, MEMS or glass based devices in a single package.

In terms of the assembly process, eWLB is well established with proven manufacturing yields. There are still some challenges in the TSV interposer assembly process flow as well as reliability/yield issues in multi-chip assembly with thin TSV interposers. From a test viewpoint, extended eWLB has a number of advantages in final testing such as handling, logistics and compatibility of current test environments.

Figure 3. 2.5D interposer approach with eWLB technology. eWLB provides a 2.5D integration platform superior to conventional TSV Interposer based solutions in overall cost and process simplicity.
Figure 4. Schematics of (a) flip chip packaging and flip chip eWLB with decoupling capacitor for a high performance application; (b) capacitor on substrate and (c) capacitor embedded in flip chip eWLB.

Flip chip eWLB

As advanced technology nodes move beyond 28nm, there are more challenges in flip chip assembly with smaller bump pitches and ELK (extreme low-k) materials in ILD (interlayer dielectric materials) structures in a device. Standard flip chip assembly needs to address bump structure/materials, UBM designs, underfill processes/materials as well as substrate materials and package design to secure good solder joint reliability with flip chip bump interconnects.

Flip chip eWLB provides a fan-out area that has a larger pad pitch and RDL layer, providing an I/O reconfiguration that minimizes substrate layer numbers while optimizes electrical performance such as combined power and ground. As shown in Figure 4 (c) and Figure 5, flip chip eWLB has the option to integrate a decoupling capacitor and place it closer to the device for better electrical performance.

Figure 5. (a) Embedded decoupling capacitors and discrete SMDs with Si device in eWLB carrier and (b) X-ray image of SMD embedded eWLB from (a); the black area in the peripheral represents for decoupling caps and SMDs, dark gray in center is for Si device.

SUBSTRATE DESIGN OPTIMIZATION WITH COMBINING eWLB TECHNOLOGY

eWLB technology has fine line width and spacing capability of 10um/10um as well as lower intrinsic electrical parameters, providing flexibility in routing designs as compared to substrate technology. Figure 6 shows the package routing design with eWLB (2-L RDL) for 4-layer (1-2-1) substrate. This was verified by a signal integrity study for high speed digital applications which included simulation and a functional test that proved a 2-L RDL eWLB design is comparable to at least 4-layer substrate designs.

Figure 6. Design optimization with (b) 2-layer RDL in eWLB for (a) 4-layer organic substrate.

With the superior electrical performance of eWLB, it is possible to reduce the number of layers in organic substrates. As shown in Table 2, a 14-layer flip chip substrate would be replaced by an 8-layer substrate with flip chip eWLB technology. There are several variables in a flip chip substrate design such as Cu trace line width/spacing, substrate thickness, via
pad and via hole size as well as flip chip/solder ball pitch. eWLB converted designs should be approached with more actual data to meet electrical performance and signal integrity. eWLB RDL designs provide an optimized and efficient signal integrity in interconnection routing with a coarse bumping pitch. With this coarse bump pitch in flip chip eWLB, we expect a lower cost organic substrate having a large pad pitch and reduced number of metal layers.

A previous study [5] shows a comparison of parasitic values of RLC for fcBGA and eWLB at 1GHz. For resistance, eWLB has 68% less value than fcBGA. Moreover, eWLB has a 66% less inductance value and 39% less capacitance value as compared to fcBGA. This is mainly due to the shorter interconnection in an eWLB package. For fcBGA, there are flip chip solder bumps and substrate interconnections that all contribute to signal delay. eWLB has shorter interconnections with the RDL process, thus it has improved electrical performance over fcBGA. Even in unit parasitics, eWLB has lower resistance and inductance values than fcBGA at all frequencies. eWLB shows less reflection noise and better transmission performance than fcBGA over all frequency ranges. fcBGA has a resonance near 7.5~8GHz due to the mutual factor of inductance and capacitance elements. This resonance affects crosstalk of neighbor signal, signal distortion/reflection, power integrity, signal integrity as well as EMI/EMC. However, eWLB shows no resonance and better electrical performance, therefore, eWLB can be applicable for higher frequency applications.

Table 2. Flip chip eWLB approach with less number of layers of organic substrate.

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<tr>
<th>Flip chip PKG</th>
<th>Flip chip eWLB</th>
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<tr>
<td>flipchip</td>
<td>eWLB (2-layer RDL)</td>
</tr>
<tr>
<td>Organic substrate (14-layer)</td>
<td>Organic substrate (8-layer)</td>
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**ENHANCED SOLDER JOINT RELIABILITY WITH RDL IN EXTENDED EWLB/FLIP CHIP EWLB [6]**

In this study, two different interconnect schemes of direct bump and RDL approaches were studied with mechanical simulation as shown Figure 7. Shearing force was simulated for each bump case. Figure 7 and Table 3 show the results from FEM (Finite Element Method) mechanical simulation. According to the results, the overall stress level was much higher in the direct bumped model. When it comes to a Cu / ELK ILD stacked area, an RDL approach produces a smaller stress value that is approximately 30% of the direct bump. The RDL approach was more stable and safer than direct bump with respect to the bump shearing condition. In this case, the additional dielectrics layers in an eWLB RDL provide stress relaxation and pad rerouting, resulting in lower stress on the ELK ILD area. As a result, better interconnection reliability can be accomplished with the RDL approach in eWLB technology.

Table 3. FEM results for maximum stress at solder bump and Cu/ELK ILD stacked area for direct bump and RDL model.
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<tr>
<th>Simulation Models</th>
<th>Max. Shear Stress (MPa)</th>
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<tr>
<td>Direct C4-bump</td>
<td>114.2</td>
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<tr>
<td>C4-bump on RDL</td>
<td>25.9</td>
</tr>
<tr>
<td>Cu column on RDL</td>
<td>27.12</td>
</tr>
<tr>
<td>ELK ILD @ Direct C4-bump</td>
<td>151.2</td>
</tr>
<tr>
<td>ELK ILD @ RDL-C4-bump</td>
<td>8.97</td>
</tr>
<tr>
<td>ELK ILD @ RDL-Cu column</td>
<td>3.529</td>
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</table>

As shown in Figure 8 and Table 3, there is a significant reduction in Von-Mises stress and shear stress in the RDL approach as compared to direct bump on die pad. Therefore, the RDL bump in eWLB packages are also a promising approach to improving package reliability of Cu/ELK interconnects in flip chip packaging. Figure 9 shows the FEM simulation results of Figure 7(a) and Figure 7(c). With RDL layers, bump stress does not directly affect ELK stack layers, therefore, there would be less mechanical damage as compared to standard flip chip bump.

**Figure 7.** Schematics of bump models for mechanical simulation. (a) C4 bump on ELK ILD stack, (b) C4 bump on RDL and (c) Cu column on RDL.

**Figure 8.** Plot of comparison of stress on bump and ELK ILD with different interconnect schemes of Figure 6.

**Figure 9.** FEM mechanical simulation results for (a) directed C4 bumped (Figure 7(a)) and (b) bump on RDL approach (Figure 7(b)).

**IV. CONCLUSIONS**

eWLB is a proven cost-effective manufacturing technology and is a versatile platform that is well-suited for a multitude of complex and highly integrated solutions that portable and
mobile applications require. The advantages of eWLB include a multi-die package design, thin 3D solution, higher performance from reduced interconnect lengths, ultra fine pitch capability and superior warpage control.

Extended eWLB and flip chip eWLB technology provide a proven integration platform as well as a lower cost solution without sacrificing electrical performance. Extended eWLB can be an alternative solution for 2.5D TSV interposer technology for mid/low-end applications. Flip chip eWLB provides a cost-effective solution with a reduced number of layers and a more relaxed design rule in flip chip substrates. In addition, eWLB provides enhanced bump solder joint reliability with an RDL approach for advanced node Cu/ELK flip chip devices.

eWLB will provide more exciting developments in the future as the scalability of its carrier size will drive greater cost effectiveness. Extended eWLB and flip chip eWLB technology are successfully enabling semiconductor manufacturers to provide the smallest, highest-performing semiconductors to meet the ever increasing demands of the converging products in the market today and in the future.

ACKNOWLEDGEMENT
Authors appreciate Jang Tae Hoan, Kim Kyung Eun, Song Hyun Jin, Park Soo Han and Dr. Liu Kai in design and characterization team, STATS ChipPAC for design optimization study, electrical simulations and characterization study of eWLB technology.

References