“Comparisons of Interfacial Reaction Characteristics on Flip Chip Package with Cu Column BOL Enhanced Process (fcCuBE®) and Bond on Capture Pad (BOC) under Electrical Current Stressing”

by

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Comparisons of Interfacial Reaction Characteristics on Flip Chip Package with Cu Column BOL Enhanced Process (fcCuBE®) and Bond on Capture Pad (BOC) under Electrical Current Stressing

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Abstract An innovative packaging solution, Flip Chip with Copper (Cu) Column bond on lead (BOL) Enhanced Process (fcCuBE®) delivers a cost effective, high performance packaging solution over typical bond on capture pad (BOC) technology. These advantages include improved routing efficiency on the substrate top layer thus allowing conversion functionality; furthermore, package cost is lowered by means of reduced substrate layer count and removal of solder on pad (SOP). On the other hand, as electronic packaging technology develops to meet the miniaturization trend from consumer demand, reliability testing will become an important issue in advanced technology area. In particular, electromigration (EM) of flip chip bumps is an increasing reliability concern in the manufacturing of integrated circuit (IC) components and electronic systems. This paper presents the results on EM characteristics on BOL and BOC structures under electrical current stressing in order to investigate the comparison between two different typed structures. EM data was collected for over 7000 hours under accelerated conditions (temperatures: 125°C, 135°C, and 150°C and stress current: 300 mA, 400 mA, and 500 mA). All samples have been tested without any failures, however, we attempted to find morphologies induced by EM effects through cross-sectional analysis and investigated the interfacial reaction characteristics between BOL and BOC structures under current stressing. EM damage was observed at the solder joint of BOC structure but the BOL structure did not show any damage from the effects of EM. The EM data indicates that the fcCuBE® BOL Cu column bump provides a significantly better EM reliability.

Keywords: fcCuBE®, Bond on lead (BOL), Bond on capture pad (BOC), Reliability, Electromigration (EM)
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1. INTRODUCTION

STATS ChipPAC developed the low cost flip chip technology utilizing Copper (Cu) column interconnect with Bond-on-Lead (BOL) pad known as fcCuBE®. This fcCuBE technology has been further developed with outstanding improvements in materials, structure and process area. [1] The application of a Cu column interconnect in place of flip chip solder bumps offers a number of benefits such as bump pitch reduction, possible design rule relaxation by using wider lines and spaces for signal routing in a given design, removal of tight solder registration requirements and removal of the solder on pad (SOP) process on the substrate, all of which result in a low cost flip chip package solution. [2] As the demand for higher current densities increases, the electronics industry continues to scale down to smaller geometries while requiring more functionality and higher performance in a device. [3] This trend leads to higher current densities and temperatures which can cause electromigration (EM)-induced electrical failure in flip chip bumps. Recently, characteristics related to EM failure in flip chip bumps have become an important reliability issue related to several important aspects such as the Joule heating effect, current crowding, Kirkendall voids formation,
intermetallic compounds (IMCs), and thermomigration caused by the unique geometry, structure and material systems used in the flip chip bump process. [4] Since EM reliability is directly related to interconnect sizes and metallurgies, new interconnect developments in the packaging industry need to be characterized for EM reliability. Many researchers have published copper column EM data with SMD pads but more study is necessary on EM results for the BOL and BOC pads. Therefore, in this study, an EM test of BOL pad types was performed under various stressing conditions and EM characteristics were compared between BOL and BOC structures. An EM test on BOC was also conducted at the same condition as BOL. This paper discusses in detail the EM results with respect to the overall analysis.

2. EXPERIMENTAL

The device design used in this test was 40nm silicon with peripheral array bumps, one trace with a 150µm pitch and two traces with a 175µm bump pitch. The package body size was 17x17 mm with 425 solder balls, 0.35 mm diameter and 0.8 mm pitch in a four layer plated through hole (PTH) substrate. The die size was approximately 5.2 x 5.7 mm. Low coefficient of thermal expansion (CTE) material was chosen as the substrate core material to control the package warpage/coplanarity in addition to providing extreme low-k (ELK) die protection. The gap between the bump nearest to the trace is the key for the fcCuBE® design. Too narrow of a gap can cause assembly related issues such as solder bridging, shorting, etc. The bumping process included polyimide (PI) re-passivation, thallium (Ti)/Cu under bump metallization (UBM), and Cu column plating with a tin (Sn)-1.8 silver (Ag) solder cap on top. As a result of this bumping structure, the peripheral bumps were located on the aluminium (Al) pads while the center mechanical bump array was located on the top passivation layer with no electrical contact. The current flow in and out (pushing through three bumps and out one bump) was designed in such a way so the substrate side failure by electron migration can be captured in an actual EM test. [1] Figure 1 shows the typical EM bump schematic for the three to one current flow condition. The electrical resistance on bumps of the BOL and BOC structures was measured using a 4-point Kelvin technique for high precision, as shown in Figure 1. Three different temperatures (125°C, 135°C, and 150°C) and three different applied electrical current stresses (300 mA, 400 mA, and 500 mA) were used in this test for the BOL structure. In addition, an EM test for the BOC structure was also conducted under the same condition of 125°C temperature and electrical current of 500 mA in order to compare the EM characteristics of BOL and BOC structures with a sample size of 12 devices under test (DUT) per each condition, as shown in Table 1. Both BOL and BOC current densities were calculated with UBM and Cu pad area per each condition as shown in Table 2.

![Figure 1. Typical EM Bump schematic for Flip Chip with Copper Column bond on lead (BOL) Enhanced Process (fcCuBE®).](image)

Table 1: Test matrix for BOL and BOC bumps

<table>
<thead>
<tr>
<th>Temp. (°C)</th>
<th>I (mA)</th>
<th>125</th>
<th>135</th>
<th>150</th>
<th>125</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>400</td>
<td>fcCuBE w/ nominal BOL pad</td>
<td>12</td>
<td>12</td>
<td>fcCuBE w/ BOC pad</td>
<td></td>
</tr>
<tr>
<td>300</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Table 2: Current densities used in test](image)

<table>
<thead>
<tr>
<th>Units</th>
<th>Applied Current</th>
<th>BOL Slde</th>
<th>Cu Pad side</th>
</tr>
</thead>
<tbody>
<tr>
<td>Types</td>
<td>Current Density</td>
<td>Cu Pad current Density</td>
<td>Cu Pad current Density</td>
</tr>
<tr>
<td>300 mA</td>
<td>9.1 x 10^3</td>
<td>7.4 x 10^3</td>
<td>4.3 x 10^3</td>
</tr>
<tr>
<td>400 mA</td>
<td>1.2 x 10^4</td>
<td>9.9 x 10^3</td>
<td>5.7 x 10^3</td>
</tr>
<tr>
<td>500 mA</td>
<td>1.5 x 10^4</td>
<td>1.5 x 10^4</td>
<td>7.1 x 10^3</td>
</tr>
<tr>
<td>BOL (5mm)</td>
<td>1.5 x 10^4</td>
<td>1.5 x 10^4</td>
<td>8.4 x 10^3</td>
</tr>
<tr>
<td>133 um (Pad dia)</td>
<td>3.6 x 10^3</td>
<td>3.6 x 10^3</td>
<td>3.6 x 10^3</td>
</tr>
</tbody>
</table>

The results demonstrated that the actual device temperature is critical when the EM test is performed. The device temperature will be greater than the oven temperature during stress due to the stress current and the effects of Joule heating; therefore, oven temperature is not an adequate measurement of device temperature. Actual temperature, including the Joule heating effect, must be measured. The temperature measurement of the device can be accomplished in several ways. In this study the actual temperatures of each DUT, especially at the local bump locations, were derived by considering the temperature coefficient of resistance (TCR) method. The average temperature increment due to Joule heating is therefore experimentally determined. As an example, Figure 2
shows a representative TCR result of the BOL structure at test with the condition of 150°C and 500 mA. The red box in Figure 2 shows the TCR value and Joule heating on one DUT while the blue box shows the average Joule heating on all DUTs. Joule heating values of all the test conditions were less than 3°C.

![Fig. 2. Representative TCR plot on BOL structure at test conditions of 150°C and 500 mA.](image)

The EM failure criterion was defined as the time at which a 15% increase in electrical resistance was observed and EM data was collected for over 7000 hours under accelerated conditions as indicated in Table 3. All samples have been tested without any failures for over 7000 hours, however, we searched for morphologies induced by EM effects through cross-sectional analysis and investigated the interfacial reaction characteristics between BOL and BOC structures under current stressing. The bump microstructures used in this test were observed with scanning electron microscopy (SEM) in the backscattered electron (BSE) mode, and the compositions of the resulting IMCs were measured by energy dispersive spectrometry (EDS).

### 3. RESULTS AND DISCUSSION

Figure 3 (a) and (b) show cross-sectional images of the fcCuBE® Cu bump and Sn-1.8Ag solder cap along with BOL and BOC structures used in this study. There are two major differences between BOL and BOC structures. The first difference is solder volume. Due to the removal of the SOP process on the substrate, the BOL structure had a smaller solder thickness than the BOC structure. The second major difference is pad type. The BOL structure has an oblong shape for the pad while the BOC structure has circular pad shape. During reflow processing, Ni-Sn IMCs (Ni<sub>3</sub>Sn<sub>4</sub>) were formed at the bonding interface between the Ni layer (diffusion barrier) and solder, and Cu-Sn IMCs (Cu<sub>3</sub>Sn<sub>5</sub> & Cu<sub>3</sub>Sn) were formed at the bonding interface between Cu pad and solder. In both cases, isolated Ag<sub>3</sub>Sn IMCs were formed inside the solder bumps, as shown in Figure 3 (a) and (b).

![Fig. 3. As-reflowed BSE micrograph cross section each structure: (a) BOL and (b) BOC.](image)

**Resistance behaviors with stress time**

Figure 4 (a)-(e) shows the resistance behaviors of BOL bumps under 5 stress combinations, as shown in Table 1. Even though test is conducted for over 7000 hours (hrs), the resistance variation per each condition was less than 3% for up to approximately 7000 hrs. From Figure 4, the excellent endurance during EM test in the BOL structure of the fcCuBE® package could be confirmed.

![Fig. 4. BOL resistance behaviors on each test condition during 7000 hrs: (a) 500 mA @ 125°C, (b) 500 mA @ 135°C, (c) 300 mA @ 150°C, (d) 400 mA @ 150°C, (e) 500 mA @ 150°C.](image)
Cross-sectional analysis: 5 stress combinations

Figure 5 (a)-(e) shows cross-sectional images on each bump of interest tested by the 5 stress combinations shown in Figure 4 (a)-(e), respectively. For all BOL bumps in Figure 5, the solder phase is completely transformed into the IMC phase during EM test and bump of interest per each condition did not show any electrical and micro-structural degradation. Massive IMC growth was observed related to the direction of the electron flow. When electrons flow from the bottom substrate side to upper Cu column side, Cu-Sn IMC (Cu₅Sn₃ & Cu₃Sn) formation is enhanced at the interface between BOL pad and solder by consuming Cu pad atoms of BOL pad. On the other hand, the Ni diffusion barrier on the Cu column side was not consumed during EM test. In addition, Kirkendall voids were observed at the Cu pad/Cu₅Sn IMC interface. It has been reported that Kirkendall void formation mechanism can be ascribed to the different diffusivities of Cu and Sn. [5] Figure 5(f) shows the bump image tested for over 5000 hrs under a higher condition of 650 mA and 160°C by a third party vendor. The resistance variation was less than 3% up to about 5000 hrs as well. The higher condition of 650 mA and 160°C also showed very stable form with no EM damage. This means that the excellent endurance for EM in BOL structure could be confirmed again. In the case where there is a limited amount of Sn, once the solder is rapidly transformed in IMCs, there was no longer any solder present to react with an infinite supply of Cu pads. For the Cu column bump, the full IMC phase is believed to be main course of the outstanding EM performance and the Cu BOL bumps are no longer expected to fail in testing conditions. Many researchers have found that full IMCs help to make the EM reliability strong with no failures. [6-7]

To investigate the IMC growth behaviour with the 5 stress combinations used in this test, the IMC area was quantified by cross-sectional SEM images and an image analyzer program, as shown in Figures 6 and 7. The IMC thickness was defined by dividing the area of the IMC by the interface length. Figures 6 and 7 show the IMC growth behaviours measured by three different current conditions and three different temperature conditions, respectively. They show very similar IMC growth. With all of them, the growth of Cu-Sn IMCs (Cu₅Sn₃ & Cu₃Sn) increased for 7000 hrs under accelerated conditions and accordingly, the solder phase was ultimately transformed into the IMC phase as mentioned above. Finally, the Cu pad was visibly consumed according to the electron direction. As shown in Figure 5, cross-sectional images also show very similar morphologies with each current stressing and temperature condition. The highest condition used in this test, 500 mA and 150°C combination, showed bigger interfacial reaction than other conditions. The higher resistance change, IMC growth and Cu pad consumption were observed with higher current and temperature conditions.
The IMC growth mechanism in this system is illustrated in Figure 8. As shown in Figure 8, during reflow processing, Ni-Sn IMC was formed at the bonding interface between the Ni layer and solder, and Cu-Sn IMCs were formed at the bonding interface between Cu pad and solder. During EM testing, the thickness of the Cu₆Sn₅ IMC increases until almost all Sn in the solder is consumed. After that, since BOL has a limited amount of Sn and an infinite supply of Cu, Cu₃Sn IMC starts to grow thicker at the expense of Cu₆Sn₅ IMC. Basically, when one molecule of Cu₆Sn₅ is converted into Cu₃Sn, it releases three Sn atoms which will in turn attract nine Cu atoms to form Cu₅Sn₃. [8] On the other hand, even though Ni₃Sn₄ IMC was formed at the interface between Ni/Sn after the reflow process, the Ni layer was not fully consumed during the EM test. This means that the Ni₃Sn₄ IMC barely grew; therefore Cu-Sn IMCs can be predicted as major IMCs inside solder.

**Diffusion of Cu is difficult due to Ni layer**

**IMCs growth : Cu/Sn > Cu/Ni/Sn**

**Ni layer is almost not consumed during EM test**

**EM damage, as shown in Figure 10 (b). In the BOC structure, it has sufficient Sn due to the SOP process and limited Cu pad system compared with limited Sn and sufficient Cu pad system of BOL (Figure 10 (a)). During electrical current stressing, the Cu₃Sn IMC was observed at the interface between solder and Cu₆Sn₅ IMC. The solder phase was almost transformed into the Cu₆Sn₅ IMC phase, therefore the bump was dominated by Cu₆Sn₅ IMC growth due to an infinite supply of solder.**

**BOL vs. BOC structure**

To compare EM characteristics between BOL and BOC Cu pad structures, an EM test on the BOC structure was conducted under the same condition of 125°C and 500 mA. Figures 9 and 10 show the resistance change of BOC structure after 7000 hrs and cross-sectional BSE micrographs for comparison of the two different pad types, respectively. Since BOC samples have also been tested without any failures for over 7000 hrs, excellent endurance for EM could be confirmed as well, however, micro-structural degradation was observed by
number of Cu atoms remain due to limited solder area. In other words, the incidence of interfacial void and crack at BOC is more likely to occur at a higher rate than with the BOL structure. In the final result, BOL and BOC structures used in this test did not show any electrical failure for over 7000 hrs which means that the EM data indicates significantly better EM reliability with an fcCuBE® bump even with small BOL pad as well as a BOC package.

Fig. 11. IMCs growth behaviors with two different pad types at 500 mA @ 125°C: (a) BOL and (b) BOC.

4. CONCLUSIONS

EM test of the BOL type was performed under various stressing conditions (temperatures: 125°C, 135°C, and 150°C) and stress current (300 mA, 400 mA, and 500 mA). To compare the EM characteristics between the BOL and BOC Cu pad structure, an EM test of the BOC pad type was conducted under the same condition of 125°C and 500 mA. Some important results are summarized as follows.

- With the three different temperature and stress current conditions, there were no significant differences on the standpoint of micro-structure, however, the higher resistance change, IMC growth behaviour and Cu pad consumption were observed with higher current and temperature conditions.
- For Cu column BOL bump, after 7000 hrs of EM test, the initial solder phase was transformed to Cu-Sn IMCs (Cu₆Sn₅ & Cu₃Sn) and Cu pad was visibly consumed by electron flow. Even though test was conducted for over 7000 hrs, the resistance variation per each condition was less than 3% up to about 7000 hrs and none of the bumps showed electrical and micro-structural degradation. The excellent endurance during EM test in the BOL structure of the fcCuBE® package could be confirmed.
- Cu column BOC bump has also been tested without any failures for over 7000 hrs; however, interfacial void formation and propagation by current crowding were observed at the cathode interface between solder and Cu₆Sn₅ IMC. The Cu pad was almost completely consumed after current stressing for 7000 hrs while it remained in the solder phase. Typically, current crowding during EM test significantly occurs at the cathode edge area and also the relatively uneven consumption morphology of the cathode Cu pad will cause incremental current crowding.

REFERENCES