Meander Delay Compensation in High-Speed Digital Multilayer Packages

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Abstract

The routing of multi-trace digital signal buses in printed circuit boards often results in mismatches in the lengths of the lines. This results in mismatched propagation time, referred to as “timing skew” in a digital system. A common method that is used to compensate for this is to add meander sections of line to lengthen the signal path length. Many advanced circuit board design tools have the capability to perform this compensation automatically.

Advanced Ball Grid Array (BGA) packages are fabricated using fine-line multilayer laminate substrates or they are built up using multilayer wafer-scale processes. The design tools for these types of packages have evolved from printed circuit board tools and typically use the same methods and principles. It is very common in BGA packages for high-speed digital applications to use meander trace patterns to match the trace lengths of high speed bus interconnections either from the chip to the solder balls or between chips in a multi-chip package.

However, electromagnetic simulation of these packages shows that despite the use of these techniques to match the physical length of the traces, electrical lengths often vary by as much as a factor of two. Examples of such packages are presented and analyzed. The resulting timing skew is not a significant problem in most current applications, since the overall delay is small compared with the clock interval. But with emerging applications pushing well beyond 10Gb/s, timing skew in packages will be an important consideration.

The reasons for the ineffectiveness of meander delay compensation are discussed, and are demonstrated by some simple simulations.

Keywords: simulation, package design, high speed

Introduction

The analysis and design methodologies used for high-speed digital packages were originally developed for system-level (i.e. circuit-board) problems. As the speeds of digital systems increased, problems of signal integrity first became apparent for these physically large structures. This problem is two-fold:

One key problem is that for sufficiently high bit rates or edge transition rates, signals propagating on chip-to-chip interconnections may suffer reflections if the lines are not properly terminated. These reflections return at a later time and may interfere with subsequent bits, causing inter-symbol interference (ISI). This aspect of the problem is solved by correct design of the line dimensions and corresponding choice of terminating impedance.

The other key problem of signal integrity is related to synchronization. Often, data is transmitted from chip to chip along parallel buses that are many bits wide. For the proper functioning of the system, it is important for these signals to be launched and received approximately at the same time. This synchronization problem requires the signal propagation delay along all of the interconnections in the bus to be reasonably well matched. The simplest approach to this problem, assuming the propagation velocity of the lines to be equal, is to match their lengths.

Computer aided design tools for PCB design have been developed to address these two key problems. For delay compensation, meander patterns are commonly used to adjust the delay of signal lines in digital buses. This type of signal trace pattern inserts extra signal path length into a small physical area, so it can be used to increase the delay on lines that are otherwise shorter than other signal lines in a data bus.
As signal speeds continue to increase, the problems of signal integrity become apparent for shorter interconnection lengths. For modern high-speed digital circuits operating at multi GB/s rates, signal integrity has become a consideration even at the level of the individual chip package. The same methodologies that were originally developed for PCBs are now being used for the design of multi-layer packages.

Figure 1 shows a section of the layout for a high speed digital package made using eWLB technology [1]. This package structure has two layers of copper metallization, and superficially resembles the structure of a two-layer PCB. These types of packages often incorporate in-package power/ground planes and their linewidth and dielectric thicknesses are compatible with the fabrication of 50Ω impedance microstrip transmission lines.

The meander patterns that are highlighted in the layout were computer generated as part of the automatic routing procedure used in the package design. The layout algorithm adds these sections of meander trace to match the lengths of all of the traces in the bus to within a specified tolerance. Typically, for a high-speed data bus the lines are matched in length to within about ±10% or less. Typical line lengths in these types of small wafer-scale packages are about 5mm or less. For the expected propagation velocity of 1.3x10^10 cm/s, this corresponds to a timing difference of about ±3ps.

However, by performing electromagnetic simulation of the layout we arrive at a very different conclusion. The meander compensation for the layout is based on the assumption of constant propagation velocity. Figure 2 shows a histogram of the propagation velocities derived from electromagnetic simulation. These velocities are calculated by dividing the signal trace length by the simulated signal delay.

These results show two interesting features: The most obvious is that the effective propagation velocity shows a very large spread from line to line. In this example bus the velocities vary by ±34%. The other feature is that the effective velocity is somewhat slower than expected. In most of these lines the signals show delays in excess of what we would expect based only on their length and structure.

Figure 3 shows another example of the use of meander delay compensation, in this case for a high-speed differential signal line. In this example, there are two sections of meander lines. In one section, both lines of the differential pair follow a meander pattern to adjust the overall delay of the differential signal. In another, smaller section one of the lines has added meander traces to adjust the skew, or relative delay between the two traces of the pair.

Many emerging digital applications use high-speed differential interconnections like this ex-
ample to implement multi-lane SERDES (serializer-deserializer) interfaces. These interfaces presently operate at speeds up to 10Gbps or beyond, and often have very stringent synchronization specs.

Figure 4 shows the pair delay versus path length for a number of example differential signal traces. These examples are implemented in the same eWLB technology as in the previous single-ended example. The delay results for the single-ended lines are also shown in the same plot for comparison.

It can be seen in this figure that the differential delays show much tighter correlation with line length than the single-ended delays. The dashed line in the figure is a least-squares fit to the differential delay results. The slope of this line is the incremental delay with respect to length, and gives a propagation velocity of 1.34×10^10 cm/s, which is close to what we would expect for these lines. Note that the delay does not extrapolate to zero for zero line length – this is because the x-axis length is for the traces only, but the delay includes the transition through the solder balls.

Clearly, the mechanisms that govern the delay in the single-ended traces are quite different from those in the differential lines. The delay in single-ended lines is very poorly correlated with length, the effective propagation velocity is much lower and shows large variation from line to line.

**Current Return**

Package design tools generally focus on the layout of the signal traces, but pay little attention to the current return paths. Characteristics impedance and delay characteristics are typically calculated based on the assumption of an ideal ground plane beneath the signal lines and reasonably uniform conditions along the direction of propagation. These assumptions are usually valid for PCB designs.

Close examination of the layout shows that these same conditions are poorly met in typical multilayer packages. Power-ground net metal coverage per layer in two-layer eWLB package designs is usually about 50% of the package area, and for 4-layer laminate flip-chip BGA designs it is only about 25%. These layers are generally shared with the signal traces and vias, resulting in significant disruption and holes in the planes.

In an ideal micro-strip transmission line, signal current propagates along the signal trace and returns through the ground plane. In a uniform line, most of the return current is concentrated in the region directly beneath the signal line. Disruptions in the ground plane that are located a small lateral distance away from the signal lines, rather than directly beneath them, have minor impact on signal propagation. This is why PCBs, with relatively sparse openings in their ground planes, show good uniform propagation characteristics.

For advanced multilayer BGA packages the openings in the ground plane are much denser. Signal lines commonly lie directly above or below ground for less than half of their length. More importantly, however, there is an inherent mismatch between the scale of the signal lines and the package ball pattern that makes it nearly impossible to achieve uniform propagation characteristics.

One of the key functions of the package is to serve as fan-out interconnection, acting as the electrical interface between the very fine pitch connections on the IC and the much coarser pitch connections available on the PCB. Signal trace dimensions, which must accommodate the IC dimensions, are on the order of 10 to 20μm. By contrast, the ball pitch, which is limited by the PCB technology, is typically 400μm. Consequently, ground return currents are necessarily diverted from their ideal location directly beneath the signal line in order to pass between the package and the PCB. This diversion shows up electrically as added inductance and increased electrical delay. This is the cause of both the anomalously high delay in the single-ended lines and also of the large spread in observed delays.

In contrast, differential lines are self-referred. The signal current in the two traces of a differential line are ideally equal and opposite, so the current in one line of the pair constitutes the return current of the other line and vice-versa. Moreover, in fine-line package technologies, the traces of the differential pair are very close together over most of their length. Their electrical characteristics are dominated by the mutual interaction between the two lines of the pair, and are relatively insensitive to other
structures. Even though the ground plane may be highly disrupted and non-uniform, as long as it affects both lines in the pair in the same way, its overall effect is small. Also, since no return currents flow in the ground plane, its inductance is much less important.

**EM Simulations Studies**

To help clarify some of the issues concerning meander delay compensation, we simulated a variety of simple transmission line structures. An example structure is shown in Figure 5.

![Figure 5: Simulated transmission line structures with meander compensation.](image)

The structures shown in this figure consist of simple microstrip transmission line connections between the solder ball connections (ports 1 and 2) and the chip connections (ports 3 and 4). The package ground plane, shown in blue, connects the main PCB ground (port 2) to the chip ground connection (port 4). In the center of each signal line is a section of meander line that is used to increase the path length. The only difference in the two structures is the placement of the solder connecting the package ground plane to the PCB.

In these structures the distance between the ball and the IC connection is 2mm. The signal path linewidth is 10μm. Meander structures were added to the signal path to increase its length from 2mm to 5mm in 0.5mm increments. The dimensions of these structures are typical parameters for packages made using eWLB or multilayer BGA technologies. With the dielectric thicknesses and material properties of the eWLB process, the linewidth would be expected to result in a characteristic impedance for the lines of about 50Ω.

Figure 6 shows the simulated delay versus signal path length for the two arrangements of ground ball location. This figure shows several interesting features. First, note that the delay does not extrapolate to zero for zero line length. This occurs because of the overhead delay that is attributable to the transition through the solder balls between the package and the PCB. It can be seen in Figure 5 that the solder ball transition is physically significant in comparison with the dimensions of the line, so it is not surprising that it also contributes significantly to the delay.

Note, in addition, that the overhead delay associated with the solder ball transition is apparently dependent on the placement of the ground return ball in relation to the signal ball. This has important consequences for package design. In wide digital buses, it is common for several signal interconnections to share a common ground return connection. In such cases, each signal ball will have a different location with respect to the shared ground connection. This is one of the reasons, as observed in Figure 4, that the delay does not correlate well with signal path length.

Finally, note that the slope of the delay versus length behavior in the two cases shown in Figure 6 is nearly the same. This indicates that the incremental delay added by the meander sections is the same, regardless of the placement of the ground return path. This slope corresponds to a signal propagation velocity of 1.7X10^10 cm/s.

![Figure 6: Simulated delay versus path length for meander-compensated lines.](image)

![Figure 7: Simulated characteristic impedance versus path length for meander-compensated lines.](image)
Figure 7 shows a similar comparison of the characteristic impedance for the two cases. For long lines in which the impedance of the on-package microstrip line dominates the behavior, the impedance approaches the expected result of 50Ω. However, for more typical lengths the impedance is significantly influenced by the solder ball transition. Note in particular that when the ground return ball is placed far from the signal ball, the impedance is significantly increased.

Figure 8 shows simulated structures for a similar comparison, but in this case the ground plane beneath the meander section of the line has been removed. In actual package designs, as discussed above, the ground plane is often discontinuous and this is a common occurrence. The resulting simulation results showing delay and characteristic impedance as a function of signal path length are shown in Figures 9 and 10.

In contrast to the results for a continuous ground plane, the overall delays shown in Figure 9 show a greater delay overhead when extrapolated to zero length, but the incremental delay that is added by the added length in the meander section is much less. The effective signal propagation in the meander section is 3.7X10^10 cm/s – faster than the speed of light. This apparent violation of physics is actually an artifact of the analysis. Adding 1mm of trace length in the meander section does not necessarily result in 1mm of added distance. In fact, in the absence of the underlying ground plane the signal energy couples across the parallel sections of the meander pattern and effectively takes a short cut [2]. The net effect is that meander the meander pattern is much less effective at adding delay when it is not located above the ground plane.

The impedance results shown in Figure 10 show very different behavior from those for a continuous ground plane. With added meander compensation the characteristic impedance rises. This is because without the underlying ground plane the meander section has high inductance and low capacitance. As the length of the meander compensation is increased, its very high impedance tends to dominate the overall impedance of the interconnection.

**Discussion**

Meander length compensation is used extensively in high-speed digital package designs. A major reason for its popularity is that design tools, originally developed for board-level layout, can automatically perform the compensation. These tools have been further developed and applied to the design of multilayer packages, and the same design practices for signal integrity have been applied.

However, an underlying assumption in meander length compensation is that the signal propagation velocity is constant along the signal path. As the results of the above examples show, this assumption is not valid in all cases. Examination of actual package designs, like those shown in Figure 4, show that...
the assumption of constant velocity is invalid in most cases.

Another significant factor in the analysis of signal delays in multilayer packages is the influence of ground return solder ball placement relative to the signal ball. Because the solder ball transition between the package and PCB is physically large compared with the line cross-section and the ball-to-ball separation is often comparable to the signal trace lengths, variations in the ball placement have effects that may be much greater than the variations in line length.

The variations in signal propagation delay and the ineffectiveness of meander compensation to correct these variations have not been an issue in most designs because the packages are small. As the above results show, the delays in the package interconnections are on the order of tens of picoseconds and the variations between lines in a bus are typically on the order of 10ps. For 1GB/s signals, this variation is only 1% of the 1000ps bit interval, so it does not seriously affect timing margins. However, digital clock speeds are routinely pushing up to 2Gb/s, and show prospects for further increases. So these variations, which are not significant in most present-day applications, are likely to be a consideration in the future.

For more demanding high speed interconnections used in SERDES applications, the connections are generally differential. In these types of interconnections, meander delay compensation is much more effective.

Conclusions

Detailed analysis of package designs that use meander delay compensation show a much greater than expected spread in the delay characteristics. Lines that are matched in length to better than ±10% show ±35% variation in signal delay.

Electromagnetic simulation results show two main reasons for the ineffectiveness of the compensation: The placement of the ground return solder balls with respect to the signal balls has a significant impact on both the signal delay and the effective characteristic impedance of the interconnection. Furthermore, the incremental delay added by the meander compensation depends critically on the continuity of the ground plane beneath the meander section.

References