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# Advanced Low Profile PoP Solution with Embedded Wafer Level PoP (eWLB-PoP) Technology

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## Abstract

Current portable electronic products are driving component packaging towards 3D packaging technologies for integrating multiple memory die and application processors (AP). Among the 3D technologies, Package-on-Package (PoP) is increasingly becoming mainstream due to its flexibility of combination and sourcing. Moreover, device designs require functional integration of IC's, especially in the 3rd dimension, hence driving new technology development towards making IC components "thin and thinner".

eWLB (embedded Wafer Level Ball Grid Array) has been introduced into production to allow for higher ball count WLP, by extending the package size beyond the area of the chip. There is also great opportunity related to a 3D variation of eWLB which would allow for mounting of components or another package on the top surface with thinner profile and Package-on-Package (eWLB-PoP) technology. 3D PoP - eWLB is envisioned as an exciting technology which will open up the floodgates for system level integration utilizing very thin stacked eWLB packages as building blocks in mobile applications.

This paper reports developments that are aimed to extend the low profile PoP application with eWLB + PoP technology. Test vehicle is designed and fabricated to demonstrate to be thin and 3D PoP solution for mobile and portable electronics. Assembly process details including laser ablation and interconnects process and mechanical characterizations are to be discussed with component and board level reliability results. Innovative package structures optimization that provide dual advantages of both form factor reduction and enhanced package reliability are reported. To enable higher interconnection density and signal routing, package with multi layer redistribution (RDL) and 10um/10um line width/spacing is fabricated and implemented on eWLB platform. Successful reliability characterization results on low profile PoP package configurations are reported that demonstrate eWLB-PoP as an enabling technology for miniaturized, low profile and cost-effective 3D PoP.

## Introduction

In just one decade hand phone has transformed from a simple communication device into more complex system integrating features that allow customers to use it as a multipurpose gadget. The carrier technology has jumped from 1G to 3G,3.5G, LTE changing at the rate of every two years and with room for potential growth with global adoption. Moving forward with this trend, packaging semiconductor devices for handheld electronics has become more challenging than ever before. Growing mismatch in interconnect gap, adding different functional chips for different features and application in similar system footprint and package size reduction to increase battery size for extended usage has opened the window for innovative embedding packaging technology.

To meet the above said challenges eWLB was developed [1] which offers additional space for routing higher I/O chips on top of Silicon chip area which is not possible in conventional WLP or WLB. It also offers comparatively better electrical, thermal and reliability performance at reduced cost with possibility to address more Moore [decreasing technology nodes with low-k dielectrics in SoC] and more than Moore [heterogeneous integration of chips with different wafer technology as SiP solution in multi die or 3D eWLB approaches].

eWLB technology uses a combination of front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer, which can greatly reduce manufacturing costs. Its benefits include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count, maximum connection density, as well as desirable electrical and thermal performance. It also offers a high-performance, power-efficient solution for the wireless market[2].

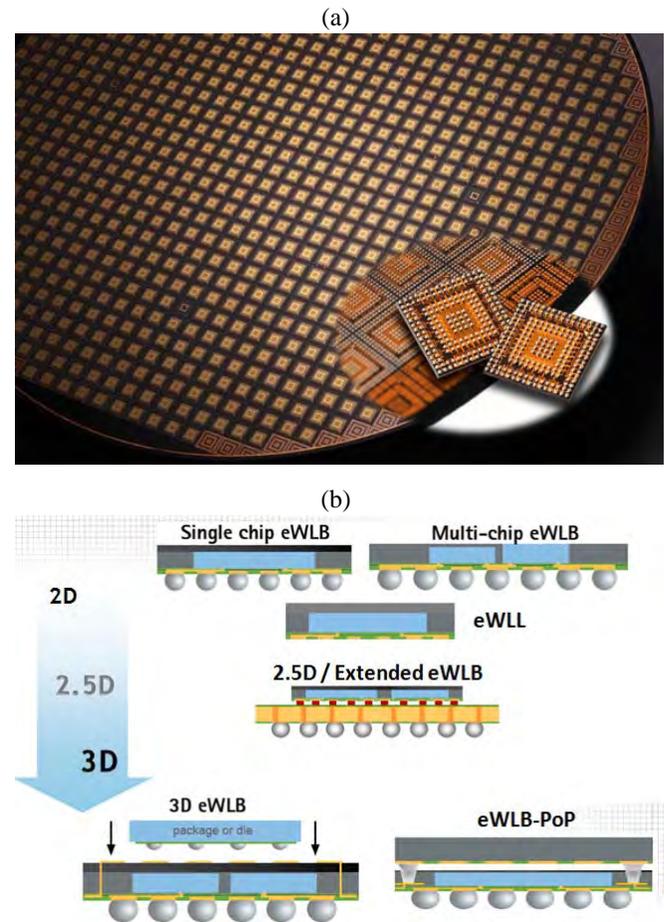


Figure 1. (a) 300mm eWLB carrier and eWLB packages, and (b) evolution of eWLB technology from 2D to 3D packaging solution

## II. eWLB-PoP Technology

The continued demand for higher level of integration has led to the industry's adoption of 3D packaging technologies and, in particular, the Package-On-Package (PoP) configurations. This technology allows for vertical integration of the memory package and the logic package into one stacked package. The top package is primarily a memory module including some combination of Flash and SDRAM, while the bottom package typically contains the logic die, which is a baseband or an application processor of some kind. Top and bottom package are connected via the pads that are located on the top side of the bottom PoP package, and these pads are used to connect the top PoP (memory module) Ball Grid Array (BGA) solder balls to the bottom PoP package. There are various PoP package types including bare-die PoP, Embedded Solder On Pad (eSOP) PoP, and Laser-Via PoP that have proliferated to meet the increasing market demand. [4]

eWLB-PoP is proprietary packaging technology using fan-out wafer level packaging (eWLB) for a lower package and vertical integration of an upper PoP package yielding significant advantages in its overall profile and cost compared to current PoP technologies. eWLB-PoP is designed to meet the lower profile PoP requirement for mobile or tablet application with cost-effective solution. eWLB-PoP bottom has less than 500um package height so total eWLB-PoP could be less than 1mm after top package stacking (body thickness of 0.45mm) as shown in Fig. 2(b). Table 1 shows value proposition of eWLB-PoP technology.

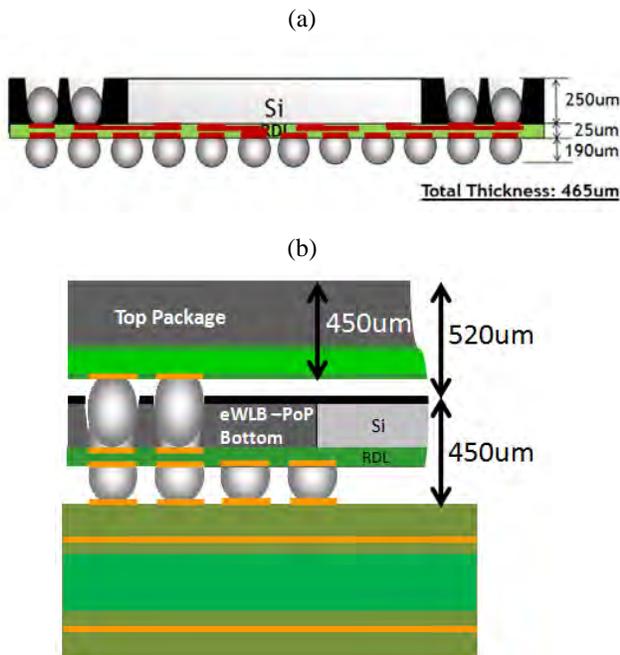


Figure 2. Schematics of package structure of eWLB-PoP ; (a) eWLB-PoP bottom package and (b) example of stacked eWLB-PoP with top package of 450um body thickness (total thickness is less than 0.1mm).

Table 1. Value proposition of eWLB-PoP

1. Thin POP solution (PoP height is < 1mm)
2. Low warpage during solder reflow cycles
3. Larger Si die cavity
4. Flexibility in memory interface
5. High routing density: L/S=10/10 (um)
6. Compatible with ELK (extreme low-k dielectric devices)
7. Good thermal performance ( $\Theta_{JA}$  18~22( $^{\circ}$ C/W),  $\Theta_{JB}$  3~7( $^{\circ}$ C/W) for 12x12mm eWLB-PoP)

### Test Vehicle Specification

For further process development and reliability tests, two test vehicles were designed as shown in Table 2. TV2 is for process development and TV1 is designed from 12x12mm fcBGA PoP products with design optimization for smaller package body size. TV1 is used for further reliability tests with ball shear and OS (open-shot) tests.

Table 2. eWLB-PoP Test vehicles specification

	TV1	TV2
Package body size	10x10mm	12x12mm
die size	64mm <sup>2</sup>	36mm <sup>2</sup>
Top ball pitch	0.4mm	0.4mm
Bottom ball pitch	0.4mm	0.4mm
Ball size	0.25mm	0.25mm
Body thickness	0.25mm	0.25mm

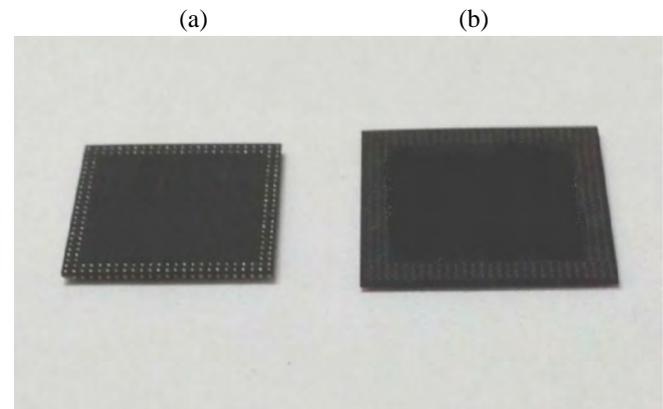


Figure 3. Micrograph of eWLB-PoPs; (a) TV1 and (b) TV2

### Assembly Process Flow

Fig. 4 shows schematics of process flow of eWLB-PoP. First, test vehicle is to assemble by eWLB process. After completion of full eWLB assembly process, then, it follows MLP process steps; laser ablation, cleaning, top ball attachment, reflow and flux cleaning, singulation and final testing. Laser ablation process was carried out to form via for solder interconnects as shown in Fig.5. SEM cross-section view of Fig. 6 shows the solder formation on laser ablated via hole.

Tapered Via shape based on larger top diameter and smaller bottom diameter helps to achieve stable solder ball loading during solder filling and stable solder heights for uniform PoP SMT stacking. A residue free Cu surface of the PoP interface lands is critical for solder wetting and PoP stacking electrical continuity. And there was no visible mold compound residue or contamination on the Cu interface lands after optimization of pad cleaning process after laser ablation.

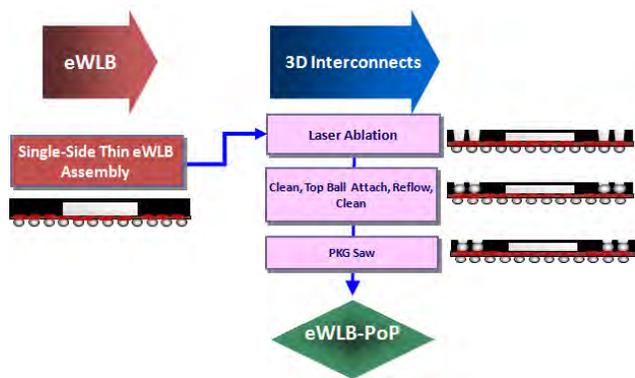


Figure 4. Assembly process flow of eWLB-PoP.



Figure 5. Micrograph of top view of eWLB-PoP, after laser ablation process to form via hole in eWLB.

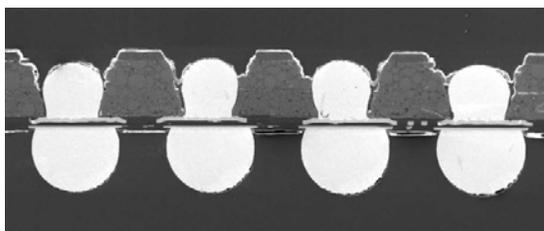


Figure 6. SEM micrograph of cross-section view of eWLB-PoP, after solder filling in laser ablated via hole.

### Component Level Reliability

Table 3 shows the package level reliability result of each next generation 3D eWLB packages. They passed JEDEC (Joint Electron Device Engineering Council) standard package reliability test such as MSL (Moisture Sensitivity Level) 1 with Pb-free solder conditions. Test vehicle (TV1) has 10x10mm eWLB-PoP. It successfully passed all industry

standard package level reliability with ball shear test and OS(open-short) test.

**Table 3. Package Level Reliability Results of eWLB-PoP packages.**

Reliability Test	JEDEC	Test Condition	Read-out	Results
Unbiased HAST (W/ MSL)	JESD22 -A118	130°C, 85%RH	168hrs	Pass
Temperature Cycling (TC-B, w/MSL)	JESD22 -A104	-55°C/125°C; 2Cy/hr	1000x	Pass
High Temp. Storage (HTS)	JESD22 -A103	150°C	1000hr	Pass

### Board Level Reliability

For board level reliability tests, eWLB-PoP (stacked with top package) was assembled and mounted on PCB as shown in Fig 7. For PoP assembly, 500um height eWLB (body thickness is 250um) top packages were assemble and total eWLB-PoP stacked package shows 750-770um height (Fig 7 and 8). Those samples were tested in JEDEC TCoB and drop reliability test conditions.

Fig. 9 and 10 show Weibull plots of 10x10 mm eWLB-PoP board level reliability of JEDEC TCoB and Drop test results. Test vehicles were PoP stacked as shown in Fig. There was TCoB first failure after 1000 cycles and its characteristic life time was 1500 cycles. Drop reliability performance was robust and showed first failure after 150 drops and its drop reliability characteristic life time was 320 drops. These test results show the robustness of board level reliability of eWLB-PoP.

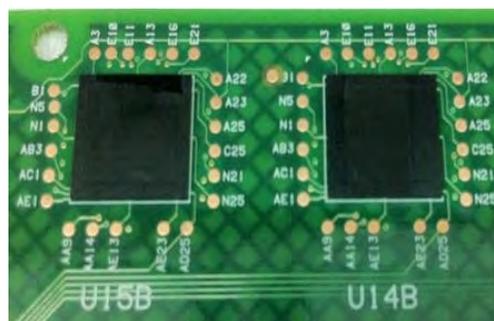


Figure 7. Board level reliability test samples of eWLB-PoP mounted on PCB

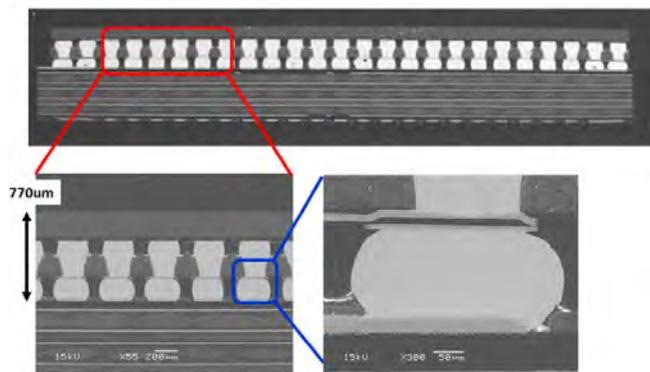


Figure 8 . SEM micrographs of eWLB after stacking 500um height eWLB top package. Total package height is 0.77mm after mounting on PCB.

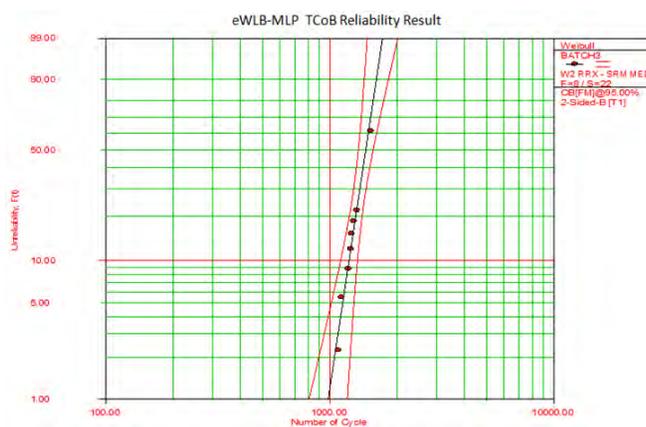


Figure 9. Weibull plot of TCoB reliability of 10x10mm eWLB-PoP (-40/125C, 2cycle/hr)

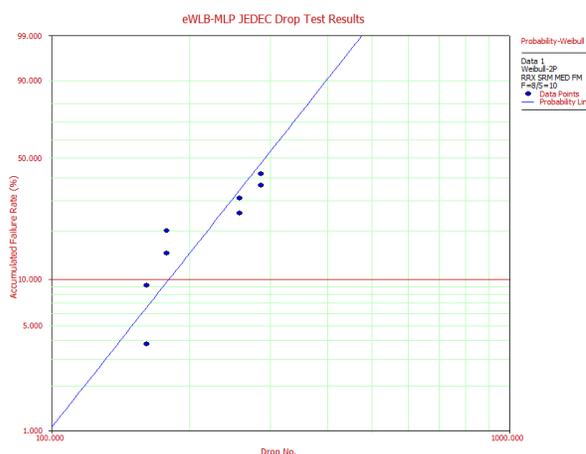


Figure 10. Weibull plot of drop reliability of 10x10mm eWLB-PoP (-40/125C, 2cycle/hr)

### Failure analysis of eWLB-PoP after board level reliability tests

In order to identify board level failure mode of eWLB-PoP, failure analysis was carried out by cross-section view observation after standard sample preparation procedure. As shown in Fig. 11, it shows solder cohesive (for TCoB test) or solder-intermetallic compound fracture (drop test) as standard failure mode reported in WLCSP or BGA packages. This proves robust package structure of eWLB-PoP with thinner package solution.

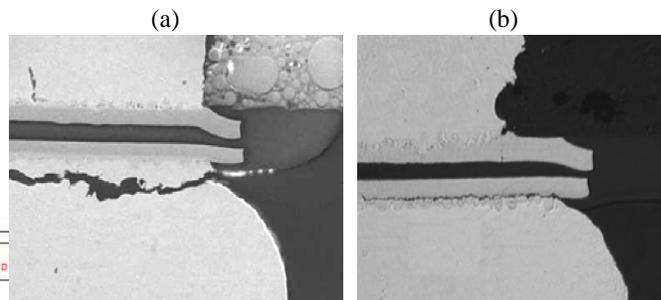


Figure 11. SEM micrographs of failure analysis of eWLB-PoP board level reliability tests; (a) TCoB : solder cohesive failure mode and (b) drop tests : IMC crack mode.

### III. Conclusions

eWLB technology is an enhancement to standard WLPs, allowing the next generation of a WLP platform due to its fan-out capability. The benefits of standard fan-in WLPs such as low packaging/assembly cost, minimum dimensions and height as well as excellent electrical and thermal performance are true for eWLB as well. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SiP), Package-on-package (PoP) and 3D stacked packaging.

PoP is configured by two individual packages resulting in a constraint to some applications due to the package thickness. A thinner product was necessary for the new generation. Currently, the overall height of PoP is approximately 1.4mm with 2-die stacked top memory package – one of the thickest components in the handset engine. Thus, low-profile PoP is crucial for further mobile or tablet, consumer applications for portability view points.

Advanced low profile eWLB-PoP was developed using a proprietary process for eWLB (fan-out WLP) and unique technology of laser ablation and solder filling. It passed JEDEC standard component level reliability conditions. PoP, package stacking and board level reliability were carried out and showed robust reliability in TCoB and drop. There would be more study on thermal, electrical performance, warpage behaviour as well as cost analysis compared to substrate-based PoP packaging.

eWLB-PoP technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of mobile/portable devices as well as 3D SiP systems.

## **Acknowledgment**

Authors appreciate Dr. Hamid ESLAMPOUR, STATSCHIPPAC INC. US, for review and valuable advices on this paper.

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