“Mixed Pitch BGA (mpBGA) Packaging Development for High Bandwidth-High Speed Networking Devices”

by

John Savic*, Mohan Nagar*, Weidong Xie*, Mudasir Ahmad*, David Senk*, Anurag Bansal*
*Cisco Systems

**STATS ChipPAC

Copyright © 2012. Reprinted from 2012 Electronic Components and Technology Conference (ECTC) Proceedings. The material is posted here by permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any STATS ChipPAC Ltd’s products or services. Internal or personal use of this material is permitted, however, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or distribution must be obtained from the IEEE by writing to pubs-permission@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
Mixed Pitch BGA (mpBGA) Packaging Development for High Bandwidth-High Speed Networking Devices

John Savic*, Mohan Nagar*, Weidong Xie*, Mudasir Ahmad*, David Senk*, Anurag Bansal*
*Cisco Systems
**STATS ChipPAC
Email: jsavic@cisco.com,

Abstract

High speed network packaging solutions have pushed the limits of known manufacturing technology into previously untested realms. Next generation ASIC’s and SiP/MCM’s are requiring packages in excess of 60mm x 60mm. These large package sizes present both significant manufacturability and reliability challenges. Developing new solutions which can adequately accommodate the needs of high speed interconnect while concurrently mitigating package size growth and the consequential reliability and manufacturability risks which result, is essential for maintaining a supply equilibrium at a sustainable cost.

This paper discusses the manufacturing process and the component reliability of a large body size (55x55mm) ASIC package TV using 40nm ELK Si technology and a Mixed Pitch Ball Grid Array (mpBGA) with BGA-side capacitance on both thin core (0.4mm) and 8+1 coreless substrates. Suitable for use at any body size, mpBGA combines tighter BGA pitch (0.94mm) and the option for BGA-side capacitance to enable optimal package decoupling and increased interconnect density. mpBGA provides a means for mitigating package size growth by inherently extending the usefulness of smaller package sizes, thereby minimizing both the package reliability risks as well as the cost associated with proving in the “next” body size up (i.e increasing from 55x55mm to 60x60mm packages). The preferred method for assembly and design of mpBGA packages on both coreless and thin core substrates will be discussed including: (1) assembly process capability, (2) preferred board level design stack-up and (3) preferred design footprint incorporating the BGA-side capacitors. A preferred BOM has been identified for the thin-core 55x55mm package which has resulted in full-pass of all relevant L1 reliability tests (MSL-4 preconditioning, HTS, uHAST and 1000TCB). Additionally, it is shown that the package co-planarity of the 55x55mm thin-core test vehicle is within the required 8 mil maximum for large body size flip chip BGA packages.

Introduction

As the “network as a platform” continues its evolution into the “cloud” supporting the convergence of various multimedia sources and collaboration tools, the demand this new technology places on the architecture, hardware, and software that makes this level of connectivity possible, pushes the limits of known technology. High-end networking and computing applications drive silicon technologies for higher data rates and increased bandwidth. The greater functionality and processing speeds required of today’s networking ASIC’s has driven flip chip packaging technology into previously untested realms of ultra-low k Si, very large package size, high substrate layer count, Pb-free solder, and thin package/core thickness. These factors are challenging existing packaging materials and assembly capability, board level assembly capability and overall package and system level reliability. In addition to these electrical and mechanical performance challenges, each subsequent “next” generation component technology requires a significant investment in time and money to assure that all the risk factors are properly allayed such that the component meets all quality and performance requirements. At the current rate at which Si node is advancing, packaging technology is refined every 2-3 years; this puts a burden on the industry to constantly “keep up” with demand for greater performance.

Package solutions need to be developed and implemented that will deliver cleaner power to the IC, provide enough I/O to accommodate the volume of high speed SERDES and satisfy all power and ground requirements without compromising reliability and cost. Furthermore, the solutions must be compatible with current PCB design rules and component assembly processes. This paper discusses the benefits and compromises of using Mixed Pitch Ball Grid Array (mpBGA) with BGA-side capacitors, defines preferred assembly processes and materials, and highlights L1/L2 reliability results.

mpBGA Test Vehicle Design

In the context of this paper, mpBGA can be defined as any configuration that varies from a traditional-orthogonal BGA pitch to accommodate specific design and performance needs. In the daisy chain Test Vehicle (TV) used in this paper, a variable 0.94mm pitch design is adopted to maximize the amount of I/O while also providing space for BGA-side capacitors. In previous work, incorporating BGA-side capacitors has been shown to significantly improve the power delivery network in high speed ASIC designs [1,2,3,4]; however, one very significant compromise is that ball count has to be reduced to accommodate placing the capacitors (~1.6 balls/per back-side 0204 cap placed) [1]. Proper use of mpBGA results in an overall increase of ball count and allows for BGA-capacitor placement (the actual quantity that can be placed will depend on die size and package size). Table 1 shows the opportunity to mitigate package size growth, add BGA-side capacitors and overall I/O for the large body die BGA TV used in this study. If added functionality, such as BGA-side capacitors is not required, mpBGA mitigates package size growth by providing more I/O per unit area; for example, a 57.5mm x 57.5mm package I/O can easily be accommodated in a 55mm x 55mm footprint. Maintaining
package sizes up to 55mm x 55mm, reduces L1/L2 reliability risk and package/PCB level assembly concerns and maintains a lower cost basis for the component.

Table 1: mpBGA opportunity for establishing more BGA interconnect and added functionality within specific BGA footprints and package body size configurations. (Ball count in "core-power" region defined by ~400mm² die)

By definition, mpBGA is difficult to standardize. In this paper a preferred mpBGA footprint was selected for evaluation with only minor adjustments to accommodate the various package sizes tested. A daisy chain TV was designed using a low ELK (40nm) daisy chain silicon die which was placed onto both thin-core and coreless substrates. The silicon is 18mm x 22mm. The 40nm Si was procured in two metallization schemes: 2MZ stack and 4MZ stack; DOE’s were set-up around each stack to assess any differences in package assembly or reliability performance.

Figure 1: Left image illustrates BGA ball configuration with BGA caps. Right and bottom images are actual assembled package (thin core – 55x55mm package).

The thin-core (0.4mm) substrate is 55x55mm, 6-2-6 stack-up fabricated using low CTE core material and GX-13 build-up. The coreless substrate is 45x45mm, 8+1 stack-up using GZ-41 - low CTE build-up material. The packages were designed with 0.5mm solder pad opening using 0.63mm SAC 305 BGA balls. Single piece lid is the preferred configuration but two-piece lid with stiffener is considered as an option in both cases if needed.

Figure 1 shows the preferred configuration. Twenty-eight 0204 (0.47µF) capacitors were placed on the back-side of the package directly under the die perimeter; forming a defacto separation between the “core-power” area and the “perimeter” outside the die shadow. The BGA-capacitors define a transition zone between two pitch configurations: the die perimeter using a 0.94mm orthogonal pitch, and the core-power area using a 0.94mm hexagonal (interstitial) pitch. In previous work [1,2,3], capacitors were placed directly under the die. L1 and L2 reliability testing was very good as were other critical parameters such as warpage, assembly yield and capacitor stand-off height (gap between capacitor on top of the PCB was shown to be typically 2-4 mils for 0204 capacitors with a nominal height of 0.3+/-.05mm) [1]. In this iteration, placing the capacitors directly under the die perimeter was chosen because it is believed to be the highest L2-interconnect stress zone. Determining the reliability impact removing BGA balls (from under the die perimeter area) will have on the adjacent BGA balls is essential in understanding how far BGA-capacitors can be placed away from the zero-stress point (center). Furthermore, this area may be important for placing AC-coupling caps on SERDES channels and thereby assessing the stress exhibited onto the capacitors (and solder joints) in this area is also critical; unlike decoupling caps which can in many cases be redundant so failures are not noticeable, AC-coupling capacitors cannot tolerate failures.

Figure 2 shows critical zones which were defined and isolated for Board Level Reliability (BLR) monitoring. The L1 interconnect (flip-chip bumps) was divided into 6 zones: defined by the die perimeter, die corner and die center area. These zones were subsequently divided into smaller regions. For example, the nine most corner bumps are monitored independently as it is believed they are likely to be exposed to the highest level of stress. And, the perimeter, which is defined as the first 10 rows of 170µm bump pitch, is divided to isolate failures from the 3 outermost rows (bump pitch is 340µm beyond the first 10 rows).

The L2 interconnect (BGA-balls) is monitored in 5 critical zones: including corner balls (zone 1), package perimeter (zone 4), die perimeter (zone 2), core power area (zone 5) and the neutral zone (zone 3). BGA-capacitors are placed in
between balls located in zone 2; the daisy chain net captures BGA-balls immediately adjacent to the BGA-capacitors in order to assess the stress displacement as described previously.

The daisy chain TV also monitors the substrate. Various micro-via and PTH chain configurations were included within the design. A high density of micro-vias was placed in die corners, die perimeter and package perimeter. In the thin-core construction, the via stack was either 2/2/2-PTH-2/2/2 or 3/3-PTH-3/3 with micro-vias placed both on and off the PTH. These constructions are monitored independently of the L1 and L2 interconnect so as to not add to complexity in case of FA. The via stack for the coreless design was slightly different (since PTH’s are not present). A typical stack-up is 2-3-3 or 3-2-3; no full stack was tested as in previous designs [2,4].

JEDEC standard package level 1 reliability tests (preconditioning with MSL-4, uHAST, 1000hr HTS, and 1000TCB (-55°C-125°C) were performed). BLR tests consist of 3500 cycles ATC (0°C-100°C), mechanical bending per IPC 9702 and mechanical shock (at 100, 200 and 340 G’s input pulse). Unified BLR test vehicle was designed as a 125 mil, 16-layer PCB board using Pb-free compatible materials and VIPPO copper. A variety of board lay-out configurations were used to assess compatibility of BGA-caps with VIPPO and define PCB design rules. At the time of writing this paper, L1/L2 testing on coreless, and L2 testing on thin core is underway. L1 reliability data for the large body size/large die, thin core package is presented in a subsequent section.

Assembly Test Plan

Thin Core Package Development Phases

Packages were manufactured at several development phases below.

Step #1 (Thermo-mechanical simulation): A numerical tool was used to understand the package interaction during assembly and post reliability conditions. Numerical results helped to select package design and the right materials to down-select the DOE (Design of Experiment). Thermal analysis was also performed to study package and system level thermal resistance, and die junction temperature for field life conditions.

Step #2 (Assembly feasibility build): One of the critical phases in manufacturing was the feasibility build with the down selected materials from simulation. Several key design parameters such as Si level structure, UBM structure, passivation type (PI over PBO), assembly process parameters, etc… were reviewed. Comprehensive DOE with assembly process parameters was conducted. Die ELK delamination and/or cracking are major concerns for 40nm die with a large die/large body size ASIC package. Robustness of the Si structure was investigated through Quick Temperature Cycle tests (QTC) for non-underfilled packages. Abbreviated package-level post reliability (multiple Pb-free reflow cycles, QTC) tests were also conducted for each material and set of assembly process conditions. Legs that passed the abbreviated package level post reliability tests, were selected for the next evaluation step.

Step #3 (Characterization build): In this development phase, die design parameters, UBM, and PI variables, substrate materials type, package BOM (Bill of Materials), lid design type and other process related parameters were fixed. Multiple good legs from the feasibility build were selected for comprehensive package reliability evaluation (limited sample size at this stage). Typical package reliability included MSL-4 preconditioning, un-biased HAST, HTS, and 1000TCB.

Step #4 (Package and Board level qualification): The final step of development is the qualification build where only the best leg from the characterization DOE was selected for comprehensive package and board level reliability (full samples size). Once comprehensive reliability testing is completed on the qualification build samples (and samples have passed), the process will be ready to scale to high volume manufacturing. Typical reliability read-points for the qualification build were EOL (End of Line) X-ray inspection, C-mode scanning (CSAM) to check for any voids, delamination or other abnormalities during assembly and accelerated test conditions, and package warpage as a function of temperature. Electrical open short testing was performed after each test item using a dedicated high volume – fully automated, test socket. Extensive failure analysis was also conducted to monitor material interface delamination, cracking, or any other abnormalities in the package.

Materials Choices

Package warpage is a big concern for large die large body flip chip packages especially those with thin core substrates. A low CTE (Coefficient of Thermal Expansion) core substrate is required for large packages with ELK die. Low CTE cores help mitigate “white bump” (WB) issues, and to reduce warpage by minimizing thermal mismatch between the substrate and die. In this study, a 14 layer substrate (6-2-6) with 0.4mm low CTE core was used. As stated previously, the thin core, 55x55mm package used GX-13 build-up whereas the 45x45mm coreless build-up package used low CTE GZ-41. The substrate was designed with proper metal balance on each layer to lessen warpage, and other potential substrate related failures in the package. One of the key design features of this study is the BGA-side mounted capacitors. Several iterations of the design and assembly process were performed to finalize the process window. A standard Pb-free device assembly process was applied in the study as shown in Figure 3.

Figure 3: Typical assembly process flow for Pb free device
40nm low ELK silicon wafers with 4MZ, and 2MZ wafer schemes with polyimide coatings were used in the evaluation. Two different underfill materials for the ELK device with high and low Tg (glass transition temperature) properties were included in the study. High Tg underfill is recommended to protect the Pb free bump whereas low Tg is for better ELK protection and package warpage control. Selecting the right underfill type for a large die package with ELK die is very challenging. High thermal conductive thermal interface material (TIM) was a must in this study because of the high-end ASIC package and expected thermal dissipation requirement for such devices. Two high conductive TIMs along with three lid seal materials were included in the study. The characterization build matrix with corresponding leg description is shown in Table 2.

A check list for various process steps during assembly was developed and monitored during the assembly process to ensure it met all required conditions. The detailed check list with monitoring methodologies is shown in Table 3.

Both TIM and lid adhesive materials are extensively characterized to meet certain requirements such as wider process window to dispense epoxy and attach lid, higher lid pull strength, low thermal resistance, etc. Both Ad-2 and Ad-3 were dropped due to much higher viscosity than Ad-1 making it very difficult to control the coverage.

<table>
<thead>
<tr>
<th>Leg #</th>
<th>Wafer and Substrate</th>
<th>BOM</th>
<th>Process Checks</th>
<th>Criteria</th>
<th>Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>4XMZ, (PI:HD4104, Core:R1515S)</td>
<td>UF-A</td>
<td>Lid pull test</td>
<td>Max. 200μm</td>
<td>Vertical gauge measurement for X, Y Diameter, Tilt</td>
</tr>
<tr>
<td>1-2</td>
<td></td>
<td>UF-A</td>
<td>Adhesive coverage</td>
<td>Min. 90%</td>
<td>Lid detach after Adhesive dispense</td>
</tr>
<tr>
<td>1-3</td>
<td></td>
<td>UF-A</td>
<td>TIM coverage</td>
<td>Min. 90% of die area</td>
<td>Lid detach after TIM dispense</td>
</tr>
<tr>
<td>1-4</td>
<td></td>
<td>UF-A</td>
<td>Warpage</td>
<td>Max. 200μm</td>
<td>Shadow Moiré measurement</td>
</tr>
<tr>
<td>1-5</td>
<td></td>
<td>UF-A</td>
<td>Final visual inspection</td>
<td>POD compliance</td>
<td>POD Compliance</td>
</tr>
</tbody>
</table>

Table 2: characterization Builds DOE

Lid pull tests were performed after EOL for all lid adhesives and TIM combination legs. Even though all legs passed the lid pull test criteria (195Kgf at 25°C), only TIM-1 and Ad-1 were selected for the qualification build due to better processability and higher bulk thermal conductivity. EOL condition package warpage was measured using Shadow Moiré tool. Table 4 shows that only relatively small warpage differences were observed across the legs. All the legs comfortably met the EOL condition package warpage requirement (< 200μm). Comprehensive package level reliability tests such as pre-conditioning with MSL-4, uHAST, HTS, and 1000TCB tests were performed. No visible difference was noticed between the wafer schemes; both were robust in assembly and reliability. The 2MZ wafer was selected for the final qualification build since it is believed to be more sensitive to accelerated life-tests and more likely to provide insight into potential failure modes.

Electrical open short (O/S) tests were performed after each accelerated test condition. Any failed units were cross-sectioned to verify failure results and failure mode. Post reliability data shows UF-A slightly outperformed UF-B, hence it was selected for the qualification build.

Table 3: Check list for Characterization DOE

Qualification Build:

The leg with the best result from the characterization build was selected for both package and board level qualification. Packages were built with 3 different lots each with 45 units. No noticeable issues were encountered in the package assembly process. CSAM results were taken on every part after the underfill cure process to make sure no underfill voids or delamination occurred in the packages. Figure 4 shows die CSAM pictures after the underfill cure process. Package level post reliability requirements were kept the same in the qualification build (JEDEC standard package level reliability tests: preconditioning with MSL-4, uHAST, HTS, and TCB). The detailed test matrix with sample size for the package level qualification build is shown in Table 5. Again, electrical open short tests were performed on every part after every readout. No failure or other degradation was observed in any of samples. Table 6 shows complete reliability data of qualification build parts.
Table 5: Package level qualification builds DOE

EOL condition package warpage data was collected using Shadow Moiré. Figure 5 shows package warpage is well below the maximum limit (<200um) at any given temperature condition. The warpage trend follows smile-to-crying as packages go from room temperature to elevated temperatures.

<table>
<thead>
<tr>
<th>EOL (after UF cure)</th>
<th>Precon L4</th>
<th>uHAST 96hrs</th>
<th>uHAST 168hrs</th>
<th>TCB 500X</th>
<th>TCB 1000X</th>
<th>TCB 5000h</th>
<th>HTST 5000h</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS test</td>
<td>C-SAM</td>
<td>OS test</td>
<td>OS test</td>
<td>OS test</td>
<td>OS test</td>
<td>OS test</td>
<td>OS test</td>
</tr>
<tr>
<td>0/135</td>
<td>0/135</td>
<td>0/135</td>
<td>0/30</td>
<td>0/73</td>
<td>0/71</td>
<td>0/30</td>
<td>28</td>
</tr>
</tbody>
</table>

Table 6: Qualification build parts reliability data

Extensive failure analyses were conducted on post reliability parts to see bump crack or other oddities in the package. X-section was done on a few parts after each reliability test. Figure 6 shows a sampling of bump images after uHAST, HTS, and TCB tests. The failure data concluded that 55X55 mm thin core large die with mixed pitch package is very robust for high end applications.

Figure 4: CSAM pictures after underfill cure

Coreless Package Characterization

There are many challenges in developing coreless large die/large body flip chip package assembly processes. One of the major challenge is to keep the bare substrate flat to fix non-wet issue during the flip chip assembly. Other issues are controlling higher package warpage in reflow condition (both assembly and post reliability process), ELK cracking during assembly due to very high CTE mismatch between the die and coreless substrate. Another issue might be BLR; again due to higher CTE of coreless substrate. The industry recognizes the important electrical advantages coreless substrates bring to high end ASIC applications and has evolved various methods to manage the warpage to within an acceptable window for high yielding assembly. Initial warpage measurements for the 45x45mm coreless substrate used in this study showed high warpage, especially at reflow conditions as shown in figure 7. A solution, utilizing a specialized BOM, was developed to manage this warpage and has yielded good assembly results. Further investigation is underway to identify the most robust and cost effective methodology for high volume manufacturing, such as: pre-attached stiffener with the substrate, magnetic boat, tape carrier substrate, etc.. to work out a suitable method and to expand the process window.

Previous work on 40x40mm coreless package size showed exceptionally good warpage, L1 and BLR results [1,2]. Equivalent results are expected as the design and assembly is optimized.

Figure 5: Final build package warpage with temperatures

In addition to evaluating various assembly techniques for attaching flip-chip die to the 45x45mm coreless substrate with warpage as depicted in figure 7, the substrate is being currently redesigned to provide a better local copper balancing within each layer.

Figure 6: Post reliability bump joint images
As stated previously, copper was balanced from layer-to-layer in both the thin core and coreless designs, however it seems evident that the thin core is capable of tolerating localized imbalance better than the coreless substrate. For the most part, the TV design was not optimized for coreless; essentially the same design is used in both package types with only minor perimeter truncation to accommodate the smaller coreless substrate.

The same plan of record for establishing a preferred BOM and assembly conditions as executed for the thin core in the previous section is outlined for the coreless substrate. Both the current non-optimized design and a new low-warpage optimized design will be built and tested simultaneously for manufacturability and L1/L2 reliability. At the time of writing, this work is not completed.

Numerical Analysis

Having completed the assembly and warpage measurements on the packages, finite element analysis (FEA) was performed, to better understand the underlying physics of the deformation patterns observed. A comprehensive new modeling methodology was developed, and used in this case to understand the deformation seen on the package and die side for each assembly process step: chip attach, underfill dispense and lid attach. Details of the new modeling methodology used can be found in a separate publication [5]. An illustration of the FEA model is shown in Figure 8. The results for the chip attach step are shown in Table 7. The use of dog-bones in the 0.94 hexagonal array with pin-field caps (assuming BGA-caps don’t offer enough decoupling) will still work but is at the outer limit of a PCB suppliers’ registration capability and assembly houses’ placement capability. Smaller PTH’s are also required and may have an inherent improvement in SI but will add further challenges to PCB house. Changes to anti-pads may be required but if hole size can be small enough and registration can be maintained, it would have little overall impact on PCB lay-out (or SI). VIPPO copper will simplify the PCB routing and registration challenges (and improve SI) somewhat but comes with a slight premium in cost. An additional consideration when using mpBGA is that signal layer routing within the BGA footprint is more complicated, especially so when signal traces must transit the hexagonal pin arrangement in the power core. It is possible that routing efficiency will be lower relative to the standard 1 mm orthogonal arrangement, and in limiting cases may require that additional signal layers be added to the design.

In order to ensure consistently high manufacturing yields and long term reliability it is necessary for the OEM to have a rigorous understanding of the target PCB suppliers’ registration capabilities, and source only from those suppliers capable of holding acceptably tight registration tolerances.

Impact of mpBGA on PCB routing requires additional consideration in order to maintain high yielding PCB manufacturability. Implicit in the 0.94 mm pitch design is that escape routing will still require two tracks between pins on signal layers and that copper webs between pins on plane layers will not be reduced. This means that registration is more challenging than it is with standard 1 mm pitch designs.

The experimental results are somewhat approximate given the different samples tested. The results show very close correlation between the experimental and FEA data. It is clear from the data that the substrate and die warpage almost double after underfill dispense. This is expected because the underfill more tightly couples the die to the substrate, resulting in higher warpage in both the die and the substrate. In the FEA model, the underfill was set at a reference temperature of 150°C, while the solder bumps were set at 220°C reference temperature. The experimental shadow moiré data was approximated at 220°C and 25°C and the difference between the two used to compare to the FEA model data. The warpage of the third and final stage of the package assembly process (lid attach and cure) shows that the lid significantly constrains the substrate and reduces its warpage by almost half, but the die warpage remains relatively unchanged.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Substrate Warpage (um)</th>
<th>Die Warpage (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Build</td>
<td>FEA</td>
<td>Build</td>
</tr>
<tr>
<td>Chip Attach</td>
<td>216</td>
<td>205.86</td>
</tr>
<tr>
<td>Underfill Dispense</td>
<td>459.6</td>
<td>425</td>
</tr>
<tr>
<td>Lid Attach</td>
<td>207</td>
<td>157.82</td>
</tr>
</tbody>
</table>

Table 7: Comparison between Experimental (Build) Data and FEA Data
Business Impact/Cost
With the rapid expansion of its flip chip technology offering and manufacturing footprint, assembly houses are positioning themselves to support the strategic growth of very large single die or multiple high end large die FlipCHIP packages with passive components which are used for ASIC devices. ASIC products are also migrating to high power with much higher density, and very stringent requirements. The cost of ASIC product development continues to grow; assembly vendor capital for product line investment grows at the same pace. Time-to-market pressures remain high, with design cycles getting shorter and market-driven product requirements skyrocketing with much cheaper price. This is one of the key challenges across the assembly vendors. Incorporating technology such as mpBGA and other Value Engineering (VE) driven technologies will sustain the growing need for higher performance ASIC’s (and other components) while sustaining a cost basis by expanding the usefulness of existing (tried and true) packaging configurations.

Conclusions
The mpBGA reliability and manufacturability evaluation has shown that the thin-core large body/ large die is very robust for assembly and performs exceptionally well through critical JEDEC level reliability testing. Coreless substrate has presented greater challenges for assembly but a plan of record which includes stiffener and rebalancing of substrate inner-layer is expected to significantly improve substrate and package co-planarity. BLR testing is planned with VIPPO Cu to assess L2 reliability with thick Cu and BGA-side capacitors and define design rules for HVM.

mpBGA effectively placates both the functional and economic requirements confronting next generation high speed network packaging solutions by enabling higher levels of functionality while concurrently delivering exceptional reliability and high yielding manufacturability.

Acknowledgments
The authors would like to thank Steven Perng and Scott Priore for their expertise in Board Level Assembly. Dr. Tae-kyu Lee for his for his expertise in forensic examination of fatigue related solder joint failures and Nguyet Anh Nguyen for her support in the PCB design. The authors want to express gratitude to the individuals at our partner companies that helped design the advanced packages; including: Joseph Dang, Lee Kim Na, Takayuki Inoue, Rick MacDonald, John Contugno, K. Sato and K. Hiyashi.

References