"eWLB Technology: Advanced Semiconductor Packaging Solutions"

by

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eWLB Technology: Advanced Semiconductor Packaging Solutions

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Introduction

The drive for small form factor and thin profile packages is being fueled by consumer and hand held electronic applications that today constitute more than 50% of semiconductor revenue. Small form factor, thin profile and cost effective technology are mandatory characteristics for packages in hand held electronic applications. Demand for Wafer Level Packages (WLP) is being driven by the need to shrink package size and height, simplify the supply chain and provide a lower overall cost by using the infrastructure of a batch process. However there are some restrictions in possible applications for fan-in WLPs since global chip trends tend toward smaller chip areas with an increasing number of interconnects. The shrinkage of the pitches and pads at the chip to package interface is happening much faster than the shrinkage at the package to board interface [1]. This interconnection gap requires fan-out packaging, where the package size is larger than the chip size in order to provide a sufficient area to accommodate the 2nd level interconnects. eWLB is a type of fan-out WLP that has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology [2, 3].

Single die eWLB packages are already in commercial volume production at multiple subcontractor packaging companies and integrated device manufacturers. However, there also exists tremendous potential for development of eWLB as advanced packaging technology that enables advanced Si node, multi-die, SiP and 3D packaging. This paper reports such developments that are aimed to extend the application space of eWLB technology. It is demonstrated in this study that eWLB packaging is compatible with integration of advanced Si node devices with low-k (LK) / ELK dielectrics. A technology envelope evaluation of eWLB is carried out where different package sizes, solder ball pitches and different Si-to-Package area ratios are fabricated & characterized. To enable higher interconnection density and signal routing, packages with multi layer redistribution (RDL) are also fabricated and evaluated on eWLB platform. Reliability characterization results on different package configurations are reported that demonstrate eWLB as an enabling technology for advanced silicon integration.

Advantages of eWLB Technology

The current BGA package technology is limited by the organic substrate capability. Moving to eWLB helps overcome such limitations and also simplifies the supply chain. Building the substrate on the package itself—allows for higher integration and routing density in less metal layers. eWLB is a next generation platform that will support future integration, particularly for wireless devices and this packaging technology has a number of important features. Transition to eWLB packaging technology enables a significant reduction in recurring costs by eliminating the need for expensive substrates. The advantage of eWLB packaging can be summarized in Table 1.

Table 1. Advantages of eWLB packaging.

| 1.  | Thinner & smaller package solution |
| 2.  | Ideal for mobile applications and meeting future roadmaps |
| 3.  | Package robustness (vs. lead-free flip chip + advanced fab nodes with ELK (extreme low-k)) |
| 4.  | Cu/low-k/ELK compatible packaging technology, Green packaging (Generic Pb-free, Halogen free) |
| 5.  | Superior board level reliability proven for mobile applications |
| 6.  | Proven lower cost path using a batch/inline process & further cost reduction with large scale panel approach |
| 7.  | Next generation eWLB technology with 3D eWLB joint development |
| 8.  | No substrate or bumping; Simple logistics and supply chain |

Advanced Si Integration in eWLB

BGA packaging also faces a challenge with technology nodes finer than 65nm as the device performance density drives the need for flip chip. But advanced flip chip nodes drive fine pitch combined with weaker low-k dielectric structures resulting in flip chip becoming narrower in terms of packaging process margin. With ultra low-k and interconnects pitch becoming smaller and smaller and with the shift to lead free materials, the technical limitations faced by the packaging industry are becoming more challenging [4]. eWLB technology provides a window for packaging next generation devices in a generic, lead-free/halogen free, green packaging scheme. Packaging of 40nm Si technology node device with ELK layers was successfully developed in eWLB.
Various process steps and methods are required to be optimized during the assembly process. Figures 1 shows 40nm silicon die images after wafer saw process. Wafer sawing of the 12 inch 40nm tech node silicon wafer with ELK layers requires laser grooving followed by step cut mechanical saw process. The metal patterns in the saw street ought to be completely removed during wafer saw process else these can lead to electrical shorts during the subsequent RDL process. The embedded die size is 3mm x 3mm, package size is 6mm x 6mm, with 144 I/O at 0.5mm pitch. Figure 2 shows cross section of RDL/device pad interface. HVM (high volume manufacturing) level assembly yields are achieved using eWLB assembly process as verified by functional electrical test. Figure 3 shows high frequency CSAM image after the assembly process. No white bump issues are detected in the eWLB unit. After assembly eWLB units were subjected to reliability tests as confirmed by functional E-tests at different read out points.

Figure 1: Si dies after wafer saw process. No ELK layer cracks or residual metal in saw street is visible

Figure 2: SEM micrograph of cross section at eWLB RDL.

Figure 3: High frequency CSAM image of eWLB unit after assembly. No white bump problem can be seen. The dark spots in the image are due to dielectric vias underneath the solder ball pad
Apart from successful 40nm Si technology node device development, eWLB packages ranging from sizes of 2.7mm – 12mm, Si-to-Package area ratio of 0.22-0.77, package pitches of 0.4-0.8mm, embedded Si device tech nodes 65, 90nm and above have also been successfully qualified.

**Small outline and extra small eWLB**

Another family of packages that is being evaluated is small fan-out and extra small eWLB. As Si nodes are migrating from 40nm to below either more and more functionality is being integrated into Si devices or for same functionality level the Si die size itself is shrinking. Thus there is need for packages that only need to be slightly bigger than the embedded Si die size. Two such packages with die sizes of 2mm x 2mm and 4mm x 4mm and package sizes of 3mm x 3mm and 5mm x 5mm respectively are successfully qualified. Both 3mm & 5mm eWLB packages have passed MSL1, TC1000X, UHAST, high temperature storage, bend, TCoB and drop reliability tests. Figure 4 shows a completed eWLB wafer with package size of 3mm x 3mm. Figure 5 shows some extra small eWLB that have been qualified. eWLB being a wafer level batch processing technology can lead to significant cost advantages for such small package sizes.

**Next generation and 3D eWLB**

Following second generation eWLB package configurations have been developed and qualified:

- Thin eWLB (250um thickness, 5mm x 5mm die, 8mm x 8mm eWLB)
- 2-L RDL (5mm x 5mm die, 8mm x 8mm eWLB)
- Multi-Chip (two-chip, 5x2.5mm, 8mm x 8mm eWLB)
- Extra Large (2-chip/3-chip, 12x12mm eWLB)
- Large (7mm x 7mm die, 8mm x 8mm eWLB / 8mm x 8mm die, 10mm x 10mm eWLB)

All these second generation eWLB variations have passed JEDEC standard based MSL1, TC850X, UHAST, HTS, 20X reflow and mobile OEM standard based drop and TCoB tests. The next generation eWLB extend the application space of eWLB by enabling different aspects of advanced packaging: (a) high density routing using 2-L RDL, (b) extremely thin profile package using thin eWLB (c) mixed signal integrated & SiP packaging using multi-chip eWLB (d) high fanout ratio embedded Si packaging using large and extra large eWLB. In the area of 3D packaging extremely thin profile eWLB is being developed for PoP applications. Figure 6 below shows details of a 5 die SiP in eWLB PoP format. PoPb has three embedded dies and PoPt has two embedded dies. Both PoPb and PoPt are fabricated in wafer level processes. No substrate is required for both top and bottom packages which results in extremely thin
Figure 6: 3D eWLB PoP is 5 die SiP. (a) Bottom package of eWLB PoP (PoPb) has 3 embedded dies (b) Cross section of eWLB PoP. Top package (PoPt) has 2 embedded dies. Total package height including solder ball is 1.3mm, which in future versions is easily reduced to less than 1mm [7].

profile of overall PoP. Improved solder joint reliability is expected because eWLB CTE is much lesser when compared to substrates, which would result in much lesser CTE mismatch between eWLB and underlying PCB [5]. As shown in Figure 7 eWLB PoPb also results in a much better warpage control over the entire reflow profile temperature range when compared to similar fcPoPb. This is due to much lesser CTE mismatch between the mold compound and embedded silicon as well as 3-dimensional well balanced structure of eWLB package. Better warpage control would result in improvement of PoP assembly and SMT yield of eWLB PoP when compared to conventional fcPoP [5].

CONCLUSIONS

Main conclusions from this work can be summarized as follows:

- eWLB is an enabling technology for advanced Si integration. Devices with 40nm Si tech node and ELK layers have been packaged in eWLB with excellent assembly yields and proven reliability. No issues of white bump or ELK layer delamination are observed.
- Small outline eWLB has been demonstrated as a viable packaging method to enable increased Si functionality integration necessitated by advanced Si technology nodes. eWLB being wafer process based batch manufacturing technology can provide significant cost benefits for small sized eWLB packages
- Several next generation eWLB variations have been developed and qualified. These next generation eWLB enable different aspects of advanced packaging like - high density routing, SiP, mixed signal integrated multi die packages and extremely thin profile packages
- 3D eWLB on eWLB (PoP) is a viable route to miniaturized PoP which, would find widespread adoption in mobile phone processors and handheld consumer electronics where small form factor and thin profile are mandatory package requirements

References


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