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(STATS ChipPAC Ltd, No.2 Woodlands Sector 1, Woodlands Spectrum 1 #01-20, Singapore 768442)

Keith Buchanan, Kath Crook, Tony Wilby, Steve Burgess
(SPTS Ltd, Ringland Way, Newport NP18 2TA UK)

shariff.dzafir@statschippac.com
keith.buchanan@spp-pts.com

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Integration of Fine-Pitched Through-Silicon Vias and Integrated Passive Devices

Dzafir Shariff, Pandi Chelvam Marimuthu, Ken Hsiao, Lily Asoy, Chia Lai Yee, Aung Kyaw Oo, Keith Buchanan¹, Kath Crook¹, Tony Wilby¹, Steve Burgess¹.

STATS ChipPAC Ltd, No.2 Woodlands Sector 1, Woodlands Spectrum 1 #01-20, Singapore 768442
¹SPTS Ltd, Ringland Way, Newport NP18 2TA UK
Shariff.DZAFIR@Statschippac.com
keith.buchanan@spp-pts.com

Abstract

This paper reports on a silicon interposer containing both Through-Silicon Vias [TSV] and Integrated Passive Devices [IPD]. The fine-pitched 30µm diameter x 100µm deep TSV connect the IPD on one side of the wafer with Re-Distribution Layer [RDL] metallization and solder bumps on the other. Such a platform provides great versatility for heterogeneous system integration and reduced form-factor packaging. Interposer manufacture is described and performance of integrated RF filters and resonators is assessed after reliability testing, including; high temperature stress, thermal cycling and accelerated stress test.

Introduction

The ongoing demand for ever-increasing functionality within electronic systems drives both CMOS device shrinkage [Moore’s Law] and integrated packaging approaches [‘More than Moore’]. Three dimensional interconnect (3D-IC) integration is an example of the ‘More-Than-Moore’ approach and offers improved system performance by reducing interconnect length to increase device speeds, and by using stacking to reduce package form factors and enable heterogeneous device integration. Use of silicon interposer provides a highly versatile vehicle for 3D integration and offers the potential to combine CMOS devices from multiple technology nodes with MEMS and photonic devices [1]. TSV is a key enabling technology for 3D-IC integration, providing low impedance contacts between adjacent tiers in the three dimensional stack [2].

Passive devices such as resistors, de-coupling capacitors, filters and resonators are key building blocks of RF circuitry but are also relatively large devices, consuming 70% or more of available board space in some cases [3]. There is, therefore, a powerful argument for combining IPD with TSV. Integrating (stacking) the passive components into the silicon interposer reduces overall package footprint and so saves space. Use of TSV reduces the interconnect length between the passive and active components, thereby reducing parasitic impedance effects and so improving system performance.

Whilst the advantages of TSV+IPD integration are clear, systems manufactured using this approach must also be reliable, and, to date, little has been published on the reliability of such systems. In this paper, we report on the reliability of a silicon interposer containing IPD and TSV. Parametric test data will be used to characterize interposer performance and will include DC and RF testing of the IPD alone and then of the IPD and TSV. Extracted S-Parameters for filters and resonators, measured before and after a variety of reliability tests demonstrate the robustness of the integrated interposer.

Process Flow

The process flow used to form the interposer is shown in Figure 1 and can be broken down into 3 stages; TSV formation, IPD formation and backside RDL/solder bump formation.

Figure 1: Steps used to form: a) TSV in Si, b) IPD on first side and c) RDL / solder bumps on second side

A silicon wafer is used for the interposer. TSV with diameter 30µm are formed in the silicon by ‘Bosch’ etching through a photo-resist mask using an SPTS Omega fxP system. The etch process is timed to stop at 135µm depth, giving vias with 4.5:1 aspect ratio. The etch process is
optimized to provide straight sidewalls, minimal bow and a scallop size consistent with the thickness of the overlying dielectric and metal layers, in this case <100nm lateral depth. It is also reported that minimizing scallop size within TSV can potentially improve reliability by reducing localized peaks in electric field [4]. Figure 2 shows post-etch SEM images of the TSV in profile and plan view.

After TSV etch, the photo-resist is stripped using oxygen plasma and etch residues are removed by wet cleaning using a commercially available formulation. Optimization of the wet clean step is essential as any residual photo-resist or polymer from the Bosch etching process will cause poor adhesion of the TSV liners.

A silicon oxide liner electrically isolates the TSV metallization from the Si interposer substrate and is deposited using a TEOS-based PECVD process in a SPTS Delta /xP system. The TEOS-based process provides ~250nm minimum sidewall coverage, combined with leakage current density of <5E-9 Acm⁻² at 2MVcm⁻¹ applied electric field and a breakdown field of >10MVcm⁻¹. Figure 3 shows SEM images of the SiO liner.

A metal stack consisting of a titanium (Ti) adhesion/barrier layer and copper (Cu) seed layer is deposited using ‘Advanced HiFill’ ionized PVD in an SPTS Sigma /xP system. Ionization of the metal enhances coverage in the lower regions of the high aspect ratio via whilst use of an cold electrostatic chuck prevents Cu agglomeration and ensures that the seed layer is continuous over the via sidewalls and base, as shown by the SEM images in Figure 4.

After PVD barrier-seed deposition, the vias are filled by Cu electroplating and the overburden removed by chemical-mechanical polishing (CMP). This completes TSV formation.

The second stage of interposer build forms the integrated passive devices above the TSV. Sputtered AlCu is patterned to form a first metal layer [M1], providing capacitor lower electrodes, signal/ground probe pads and TSV contacts. Then a first dielectric passivation layer is deposited and vias opened to the M1 pads. Inductor coils are formed in a second, thicker layer of electroplated Cu, this also serving as the upper electrode for planar Metal-Insulator-Metal (MIM) capacitors. Capacitor dielectric is less than 1µm in thickness. Finally a second dielectric passivation layer is deposited, followed by patterning and etch to open up the probe pads. The test patterns in the IPD layer include TSV continuity chains, capacitors, low-pass and band-pass filters and 1GHz and 8 GHz resonators.
After IPD formation, the wafer is flipped and bonded, face-down, to a temporary glass carrier to allow thinning of the interposer from the back side to expose the TSV. The interposer is then thinned by back-grinding and chemical-mechanical polishing to a finished silicon thickness of 100µm. At this stage, the TSV are exposed.

The third, and final stage of the interposer build adds contacts, RDL and solder bumps to the back side of the wafer. A dielectric passivation layer is deposited and this is patterned and etched to allow contacts to be made to the TSV using RDL metallization.

A second dielectric layer is then applied, through which final backside contacts are made and lead-free solder bumps formed. Finally, the completed interposer structure is debonded from the temporary carrier and diced in preparation for reliability testing. Figure 5 shows an IPD schematic [L-C filter] built with TSV and cross-sectional SEM images of the thinned interposer showing front side IPD, TSV and back side RDL.

**Test Structures and Methods**

A variety of test structures were used to assess the functionality and reliability of the interposer. Continuity was assessed by measuring daisy chains containing 232 TSV per 4x4 test die. Low-pass and band-pass L-C filters, were built and performance assessed through extraction of S-Parameters. For these devices, TSV were included in the test circuits for S-Parameter extraction. Resonators [1GHz and 8GHz] were also built and characterized by S-parameter extraction, though in this case, TSV were not included in the test circuits. Figure 6 shows a schematic of the finished interposer together with a test schematic for the filters, whilst Figure 7 shows the layouts of the 4x4 continuity test die and the low-pass and band-pass filters.

Standard IPC/JEDEC tests were used to assess reliability of the daisy chains, filters and resonators: Moisture Sensitivity Level [MSL3 – 24 hour bake at 125°C and 192 hours soak at 30°C / 60% RH followed by 3x reflow at 260°C]; Thermal Cycling [TC-B, -55°C to 125°C, 500x], High Temperature Storage Lifetime [HTS, 500 hours, 150°C] and Unbiased Highly Accelerated Temperature and Humidity [UHAST, 130°C, 85% RH for 96 hours]. For each of the tests above, the extracted S-Parameters were measured before and after. For the continuity test, daisy-chain resistance was measured before and after. For the reliability assessment, 221 dice were measured for continuity and for each filter and resonator type, 5 die were measured.

![Figure 5: a) L-C filter schematic and b) SEM image showing filter realization in Si interposer with TSV c) Magnified SEM image of TSV](image)

Figure 6: Schematic showing interposer with IPD and TSV (a) and filter test schematic (b)
Figure 7: Test structures: a) Continuity test die design; b) Continuity test structure layout; c) Low pass filter layout; d) Band pass filter layout

Reliability Test Results

Table 1 summarizes the reliability test data whilst the S-Parameter data for the low-pass and band-pass filters is shown in Figures 8 and 9 and the S-Parameter data for the 1GHz and 8GHz resonators is shown in Figures 10 and 11.

<table>
<thead>
<tr>
<th>Device</th>
<th>Measured Side</th>
<th>Measured Through TSV</th>
<th>Reliability Test Results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSL-3 30°C 60% RH 192 Hrs</td>
</tr>
<tr>
<td>4x4 Continuity</td>
<td>RDL</td>
<td>Yes</td>
<td>100% Pass</td>
</tr>
<tr>
<td>LP Filter</td>
<td>IPD</td>
<td>Yes</td>
<td>100% Pass</td>
</tr>
<tr>
<td>BP Filter</td>
<td>IPD</td>
<td>Yes</td>
<td>100% Pass</td>
</tr>
<tr>
<td>1GHz Resonator</td>
<td>IPD</td>
<td>No</td>
<td>100% Pass</td>
</tr>
<tr>
<td>8GHz Resonator</td>
<td>IPD</td>
<td>No</td>
<td>100% Pass</td>
</tr>
</tbody>
</table>

Table 1: Summary of reliability test results

Figure 8: Low Pass Filter S-Parameters before and after reliability test: a) MSL3; b) HTS; c) TC-B and d) UHAST

Figure 9: Band Pass Filter S-Parameters before and after reliability test: a) MSL3; b) HTS; c) TC-B and d) UHAST

Figure 10: 1GHz Resonator S-Parameters before and after reliability test: a) HTS; b) TC-B and c) UHAST

Figure 11: 8GHz Resonator S-Parameters before and after reliability test: a) HTS; b) TC-B and c) UHAST

The continuity tests show 100% pass for all die tested, both before and after the reliability testing. This demonstrates the robustness of the integrated interposer, especially the TSVs which have not previously been subjected to such rigorous stress testing. Similarly, the frequency responses of the filters with TSV in the circuitry show no changes after the same stress tests. The data shows that the dielectric liner deposited over the scalloped via sidewall provides sufficient...
electrical isolation and does not degrade during the stress testing. It is also assumed that adhesion of the dielectric and metal films deposited within the TSV is sufficient to survive the stress testing without major mechanical failure.

**Future Work**

The reliability testing described in the paper will continue to fully meet the test specifications [1,000 cycles TC-B, 1,000 hours HTS and 168 hours UHAST]. Additionally, the work will be extended to evaluate thinner Si interposers [~50µm] and smaller diameter TSV to meet the demand for smaller form factor packages.

**Conclusions**

Integration of IPD and TSV into a thinned [100µm] silicon interposer has been successfully demonstrated. The integrated device is a milestone achievement and enables increased system performance with reduced package footprint. Reliability test data proves the robustness of the TSV in thin substrates. The approach described opens up new packaging options for mobile applications where system packaging density must be maximized.

**References**