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Advanced Laminate Carrier Module Warpage Considerations for 32nm Pb-free, FC PBGA Package Design and Assembly

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Abstract

The trend in large body, high performance integrated circuit packaging for the 32 nm semiconductor node and beyond is towards low dielectric loss to enable high bandwidth / low loss channels, and low thermal expansion to protect fragile, ultra-low dielectric constant (k) chip dielectric materials from differential expansion stress. A low coefficient of thermal expansion (CTE), low dielectric loss laminate composite was developed using industry standard Sequential Build Up (SBU) fabrication techniques and novel laminate materials. This laminate technology was used in assembly of a Flip Chip Plastic Ball Grid Array (FC PBGA) module including a silicon test structure developed for 32 nm Custom Logic development. The same silicon test structure and laminate design were also used to fabricate modules using conventional high volume laminate materials.

Various laminate physical parameters including composite CTE were determined. The warpage shape of each laminate was initially characterized at room temperature, and over the temperature range from 25°C to 240°C. Warpage of critical package features was measured and tracked throughout the various steps of the lead free flip chip module assembly process for multiple laminate cross sections, core and build-up materials.

A quantity of assemblies of each type was built and measured, data is reported. Advantages and disadvantages of each laminate module type and implications for robust package assembly as evidenced by these results are discussed.

The Performance Challenge

Recent advancement in semiconductor technology has increased the requirement for high performance signal transmission through module and board to accommodate ever increasing channel bandwidth. High Speed Serial Link standards (HSSL) continue to establish high speed data rate targets, the current challenge being the implementation of a 25+ Gbps (Gigabit per Second)/12.5 GHz interface. Greater speeds mean greater attenuation. The need to manage attenuation in substrates challenges laminate technology to deliver composites fabricated with insulator material demonstrating significantly reduced dielectric loss at higher speed as compared to the current high volume laminate technology. This demand applies to both dielectric and conduction losses. Conductor surface roughness must also be carefully managed to deliver desired benchmark performance.

To achieve performance targets, lower k dielectric materials are used in the back end of the semiconductor line. These materials are intrinsically less mechanically robust than previous generations that utilized higher k oxide materials. These lower k dielectric materials are more sensitive to damage from stresses imposed by differential expansion between chip and substrate during reflow joining and subsequent thermal processing.

A new substrate dielectric material and process (build-up dielectric B) has been developed that offers significant potential improvements in both of these areas. Stripline total loss measurements (dielectric loss combined with conductor losses) show a reduction of 0.05 dB (decibels)/mm at 12.5 GHz as compared to an identical structure in the current high volume dielectric material (build-up dielectric A) when measured at 80°C, as shown in Figure 1. In these measurements, the identical trace design is used. Copper surface roughness using dielectric B is less than dielectric A.

![Figure 1. Differential insertion loss comparison at 80°C](image)

The low loss dielectric material is less susceptible to electrical performance variation with temperature, as shown by the plot of dielectric loss tangent in Figure 2.

![Figure 2. Temperature dependence of dielectric loss](image)
Material Selection

The high speed signal performance of the epoxy based dielectrics traditionally used in build up laminate substrates is limited by non-crosslinked polar groups appended to the polymer chain which resonate in high frequency operation, damping electrical signals [1]. Various chemical compositions and approaches are being tried by polymer compounders to deliver improved dielectric loss. These include chemical formulations with reduced non-crosslinked polar groups, as well as increased silica filler loadings. To reduce conductive losses, advanced rougheners and adhesion promoters are being developed to enable smoother copper surface finishes with good adhesion of dielectric to metal. The material chosen for the advanced carrier (build-up dielectric B) uses a cyanate ester based resin to eliminate polar groups, as well as higher filler loading when compared to the current high volume material (build-up dielectric A). This composition yields significant changes in mechanical as well as electrical properties with potential benefits in terms of module warpage and die thermo-mechanical stress reduction. Dielectric loss is reduced by more than 50%, while the CTE below glass transition temperature is reduced at a similar rate. This brings the CTE value to a near perfect match with copper (17 ppm/°C), as shown in Table 1.

Less desirable consequences include an increase in Young’s modulus and decrease in elongation to failure. Cracking of dielectric build-up B has been observed to occur before dielectric build-up A in thermal cycling stresses. Cracking of both laminate materials is expected to occur only well beyond the most strenuous use conditions.

All other laminate materials, including core plated through hole fill epoxy and top and bottom solder resist are unchanged in moving from the current high volume to Advanced Carrier compositions.

Module Design

The laminates used in this study were 55 mm x 55 mm square. Two laminate cross sections were used, a 3/2/3, consisting of three layers of build-up and copper on either side of a copper clad core, and a 5/2/5 structure, consisting of five layers of build-up and copper on either side of a copper clad core. Core thickness is nominally 400 μm, while build-up dielectric layers are in the 33 μm range. Build-up copper thicknesses are nominally 15 μm, while the core copper is 20 μm. SAC 305 (Sn-3%Ag-0.5%Cu) presolder is applied to the laminate and coined to provide a flat surface for joining.

The silicon chips used were 388 mm², 0.8 mm thick. These full thickness die are typically flat to within 2 μm at room temperature. Chip bump compositions are lead free of the tin-silver (Sn-Ag) type. Nominal bump pitch is 150 μm.

Chip joining was performed at typical lead-free temperatures (nominal peak temperature of 245°C) using a convection oven with nitrogen atmosphere. Test devices in the assemblies were underfilled using a capillary type encapsulant. Nominal underfill Tg, CTE, and Young’s modulus were 100°C, 25 ppm/°C, and 10 GPa, respectively [2]. After underfill cure, a one piece nickel-plated copper lid was applied using silicone based peripheral adhesive. Thermal dissipation is achieved with a high conductivity, filled silicone thermal interface material between the die and the lid [3]. SAC 310 BGA (ball grid array) balls were then attached using a convection reflow process to complete the module assembly. A module schematic is shown in Figure 3.

## Table 1. Typical Build-up Dielectric Material Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTE (X,Y,Z) @ 150°C</td>
<td>46</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>150-240°C</td>
<td>120</td>
</tr>
<tr>
<td>Tg (TMA) °C</td>
<td>156</td>
<td>176</td>
</tr>
<tr>
<td>Dielectric constant @ 5.8GHz by cavity perturbation</td>
<td>0.019</td>
<td>0.0074</td>
</tr>
<tr>
<td>Dielectric constant @ 5.8GHz by cavity perturbation</td>
<td>3.1</td>
<td>3.3</td>
</tr>
<tr>
<td>Young’s modulus [GPa]</td>
<td>4</td>
<td>9</td>
</tr>
<tr>
<td>Tensile strength [MPa]</td>
<td>93</td>
<td>120</td>
</tr>
<tr>
<td>Elongation [%]</td>
<td>5</td>
<td>1.7</td>
</tr>
<tr>
<td>Filler content [wt.%)</td>
<td>38</td>
<td>66</td>
</tr>
<tr>
<td>Base material</td>
<td>Epoxy</td>
<td>Epoxy Cyanate</td>
</tr>
</tbody>
</table>

## Table 2. Typical Core Material Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTE: X-Y axis @ 20°C</td>
<td>15</td>
<td>12</td>
</tr>
<tr>
<td>CTE: Z axis @ 20°C</td>
<td>33</td>
<td>30</td>
</tr>
<tr>
<td>Tg (TMA) °C</td>
<td>173</td>
<td>180</td>
</tr>
<tr>
<td>Elastic modulus [GPa]</td>
<td>25</td>
<td>27</td>
</tr>
<tr>
<td>Dielectric constant @1GHz 20°C</td>
<td>4.8</td>
<td>4.8</td>
</tr>
<tr>
<td>Dielectric Loss @1GHz 20°C</td>
<td>0.019</td>
<td>0.015</td>
</tr>
<tr>
<td>Moisture absorption [%]</td>
<td>0.06</td>
<td>0.12</td>
</tr>
<tr>
<td>Poisson’s ratio</td>
<td>0.21</td>
<td>0.19</td>
</tr>
<tr>
<td>Dielectric breakdown [kV/mm]</td>
<td>40</td>
<td>60</td>
</tr>
<tr>
<td>Thermal Conductivity [W/mK]</td>
<td>0.81</td>
<td>0.7</td>
</tr>
</tbody>
</table>

Figure 3. Module Cross-section
The composite of build-up dielectric A and core A is laminate A. Laminate B is formed similarly. Laminate composite CTE’s were characterized by digital image correlation (DIC). Laminate surface features were characterized inside the chip site and on the laminate periphery as shown in Table 3.

<table>
<thead>
<tr>
<th>Laminate Composite</th>
<th>Chip site</th>
<th>Periphery</th>
</tr>
</thead>
<tbody>
<tr>
<td>3/2/3 A build-up A core</td>
<td>18.4</td>
<td>18.4</td>
</tr>
<tr>
<td>3/2/3 B build-up B core</td>
<td>17.5</td>
<td>17.1</td>
</tr>
<tr>
<td>5/2/5 A build-up A core</td>
<td>18.4</td>
<td>18.5</td>
</tr>
<tr>
<td>5/2/5 B build-up B core</td>
<td>17.2</td>
<td>17.7</td>
</tr>
</tbody>
</table>

Table 3. Laminate Composite Material CTE (ppm/°C)

Results indicate higher CTE variation between copper rich and copper lean areas for the lower CTE materials. In general, significant changes in dielectric CTE result in only modest deviations in laminate composite CTE from the elemental copper value.

Methodology

Four measurement techniques were used to characterize laminate and module warpage shape. Room temperature techniques were: coplanarity measurement using the least squares best fit plane method [4] by a non-contact optical inspection system [5], camber by non-contact white light reflectometry [6]. Elevated temperature techniques were: warpage shape characterization by digital image correlation, DIC [7], and Shadow Moire [8]. Non-contact optical inspection was 100% while other techniques were sample. Measurements were made at various points through the chip joint process, as shown in Figure 4. Optical mapping for warpage measurement is of the entire laminate BGA side. Post processing allows segregation and independent statistical manipulation of warpage/coplanarity in the die area alone. Camber indicates characterization of the die backside only by non-contact white light reflectometry. Two full diagonal line profiles are used to generate a deformed shape for the die. DIC and Shadow Moire refers to characterization of the full laminate BGA side shape over the temperature range from room temperature to 240°C, with ability through software processing to segregate and statistically manipulate the chip site and full laminate measurements separately.

Fifty laminate/die assemblies of each type were built, comprised of a single laminate lot for each type. Die lots were mixed.

Results

Incoming laminate shape is typically concave, with curvature facing the chip at room temperature. Data shown is for the backside of the laminate shape (avoiding discontinuities caused by presolder bumps) and is extrapolated to the front by the assumption that the laminate thickness remains constant across the chip site area. Correlation of topside with bottom side data in the chip area shows a consistent shift of about 10 μm, showing the leveling effects of presolder coining. We see a general trend in shape upon incoming inspection, which shows that the degree of concavity decreases with increasing layer count and increases from Material A to B, shown in Figure 5. Overall laminate shape shows a similar trend to chip site coplanarity.

Subsequent to laminate pre-bake, samples of these laminate sets were then evaluated over the full range of temperature of interest using DIC and Shadow Moire. Shape Inversion Plots [7] were then generated illustrating the shape change of the chip site area, where the plotted value is the difference between the height of the 4 corners of the chip site minus the height of the center of the chip site. Concave shape is plotted as a positive value, while convex as negative. The thermal warpage performance of 3/2/3 and 5/2/5 cross sections for materials A and B are shown in Figures 6 & 7. These show good correlation between Shadow Moire and DIC measurement.

Figure 5. Incoming coplanarity of chip site on BGA side

Figure 6. Incoming absolute warpage of chip site by DIC
The thermal warpage behavior for the two material sets as evaluated in the same laminate design is quite different. Although the shapes of both laminates are similar at room temperature, concave, at joining temperature material set A has inverted to a convex shape, while material set B remains concave although at reduced magnitude. The implications are significant for ensuring robust chip join yields, in that a process that is optimized for a convex laminate shape at joining temperatures may not perform nearly as well for the concave condition. The opposite is also likely true.

Coplanarity and die camber were next evaluated at room temperature immediately (within 10 minutes) after chip join. Warpage magnitudes are roughly equivalent for both material sets at joining temperature, although shapes are opposite. These shapes are frozen in place during chip join. Cross section results show Material A assemblies join with high flip chip bump standoff at chip periphery, and low flip chip bump standoff at chip center. For Material B assemblies, this is reversed, with high, flip-chip bump standoff heights in the module center and low bump heights at the module periphery. These differences in standoff height roughly correspond to the contours measured by DIC/Shadow Moire at solder solidification temperatures on post-bake laminates. Die camber measurements following chip joining on 3/2/3 assemblies show higher camber for material B (Figure 8), while coplanarity measurements of chip site on BGA side show significantly higher convex warpage values for 3/2/3 A than 3/2/3 B (Figure 9). The difference between the die top and substrate bottom shapes corresponds to the difference in flip chip bump standoff height, center to edge, measured by cross section, for the two assembly types. For 5/2/5 assemblies of the 2 material sets, differences are small.

Table 4 shows the bump height values demonstrating this difference. Figure 10 shows a typical joined center flip chip bump standoff height for the Material B 3/2/3 cross-section. Figure 11 illustrates the shape differences through joining of the two material sets.

![Chip site absolute warpage by Shadow Moire](image)

**Figure 7.** Chip site absolute warpage by Shadow Moire

<table>
<thead>
<tr>
<th>Laminate</th>
<th>Chip Center height</th>
<th>Chip Corner Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material A 3/2/3</td>
<td>60</td>
<td>73</td>
</tr>
<tr>
<td>Material B 3/2/3</td>
<td>56</td>
<td>43</td>
</tr>
<tr>
<td>Material A 5/2/5</td>
<td>68</td>
<td>79</td>
</tr>
<tr>
<td>Material B 5/2/5</td>
<td>58</td>
<td>55</td>
</tr>
</tbody>
</table>

**Table 4. Standoff Height (μm) vs. Laminate Type**

![Die camber across chip diagonal on 3/2/3 laminates, post-chip join (CJ) and post-underfill (UF)](image)

**Figure 8.** Die camber across chip diagonal on 3/2/3 laminates, post-chip join (CJ) and post-underfill (UF)

![Post-chip join coplanarity of chip site on BGA side](image)

**Figure 9.** Post-chip join coplanarity of chip site on BGA side

![Typical flip chip solder joint and stand-off height](image)

**Figure 10.** Typical flip chip solder joint and stand-off height
Measurements of die camber made at process steps post chip join and underfill show chip join stresses are relaxed prior to underfill cure, while underfill stresses are locked in by cure. Post underfill cure Material B assemblies show lower coplanarity and die camber as compared to Material A (Figure 12) corresponding to the reduced CTE mismatch with silicon for B versus A.

At this stage, die camber and chip site laminate shape are fixed by underfill, while overall laminate shape continues to change with processing. Laminate shapes are all highly convex. Shape now reflects the effects of reduced CTE mismatch with silicon for the B materials, Figure 13.

Post lid attach, the benefits of the lower CTE remain apparent in terms of module coplanarity (Figure 14), but the shape is transformed from a monotonic cone to a more complex sombrero-like configuration (Figure 15). This unique shape factor is carried through BGA attach to the finished module. At the finished module level, BGA coplanarity improvement for the new materials is in the 30 μm range (20%), while the improvement for 3/2/3 cross section over 5/2/5 is in the 20 μm range (15%).

Figure 16 is a compilation of the warpage behavior of the full module, BGA side, through the various processing steps, from incoming laminates through BGA attach.

**Discussion**

Although incoming laminate warpage both chip site and full laminate for both cross sections increases with the transition from the high volume (A) to low loss (B) material sets, shape at room temperature is similar. The primary distinguishing factor between composites of these two material sets is shape at elevated temperature. Of primary interest is the shape at SAC solder solidification (less than 220°C) [9]. From DIC/Shadow Moire measurements, the
shape of A composites is concave in the chip site area, becoming convex with temperature, while B chip site composite shape is concave, with concavity decreasing with temperature. It is essentially impossible to use the same solder volume, design, and reflow parameters to optimize yields for composites A and B. Although many years of industry practice have yielded well tailored methods to produce robust assembly yields with high reliability performance of moderately convex shaped modules at joining temperature, similar results for composites displaying moderately concave at joining have yet to be developed. Ideally, design practices for low loss material composites will be modified to produce a chip site shape from flat to slightly convex at the solder solidification temperature.

Assemblies of the current design show slightly higher die camber immediately post reflow for the low loss material set evaluated. This effect can entirely be attributed to differences in laminate shape at joining temperature. High temperature shape improvements for low loss composites would yield improved die camber post joining, consistent with the reduced CTE delta between laminate and silicon as compared to the current materials in high volume production.

In downstream processing post-chip join through BGA attach, introduction of low loss, low CTE materials is entirely beneficial in terms of warpage, ultimately delivering better die flatness for consistent thermal interface, as well as BGA coplanarity for assembly at the next level.

Reliability
Assembled B modules have been subjected to the following stresses:

- Thermal Cycle condition B (-55/+125°C), 1000 cycles
- Thermal Cycle condition J (card level) (0/+100°C), 3500 cycles [10]
- HAST (highly accelerated stress test) 130°C/85%RH/3.7V bias, 96 hrs [11]
- THB (temperature humidity bias) 85°C/85%RH/3.7V bias, 1000 hrs [12]

with positive results.

Conclusion
A low dielectric loss, low CTE FC PBGA laminate composite has been developed using conventional fabrication processes and novel materials. The electrical performance enabled by this development will facilitate achievement of HSSL performance benchmarks for multiple future silicon generations. These laminates developed to meet high data rate requirements have been successfully assembled into FC PBGA modules with acceptable prototype yields. In addition to the performance benefits, introduction of these new materials results in reduced module warpage, which will produce improved module assembly yield and downstream performance.

Low layer count composites (3/2/3) of material B have a shape which differs significantly from material A laminate shapes at chip join temperature, and produce less than optimum die camber as a result. Modification of laminate design and module assembly practices are needed to optimize post-assembly die bending stresses when using these advanced low CTE low-loss materials.

![Warpage behavior through the assembly process](image)
Acknowledgments

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References