“Development of Super Thin TSV PoP”

by

Seung Wook Yoon, *Kazuo Ishibashi, Shariff Dzafir, Meenakshi Prashant, Pandi Chelvam Marimuthu and **Flynn Carson

STATS ChipPAC Ltd. 5 Yishun
n Street 23, Singapore 768442

* Nokia Japan Co., Ltd. ARCO Tower 4F, 1-8-1 Shimomeguro, Meguro-ku, Tokyo
153-0064 Japan

**STATS ChipPAC, Inc., 74700 Kato Rd., Fremont CA

Copyright © 2011.
Reprinted from 2011 Electronic Components and Technology Conference (ECTC) Proceedings. The material is posted here by permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any STATS ChipPAC Ltd’s products or services. Internal or personal use of this material is permitted, however, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or distribution must be obtained from the IEEE by writing to pubs-permission@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
Abstract

One of the hottest topics in the semiconductor industry today is a 3D packaging using Through Silicon Via (TSV) technology. Driven by the need for improved electrical performance or the reduction of timing delays, methods to use short vertical interconnects have been developed to replace the long interconnects found in 2D packaging. 3D TSV interposer is an efficient and practical approach to solving die integration challenges. Many microsystem devices that will have to move to wafer-level packages will also facilitate further integration using silicon TSV interposers.

This paper will address TSV interposer development for mobile applications to replace normal organic laminate substrate. Major driver of this work is for PoP thickness reduction since current organic PoP is one of the thickest components in cellular phone engine.

Super Thin PoP test vehicle was designed in order to prove the viability of this technology. This test vehicle was a 12x12mm package with 0.4mm ball pitch on the bottom and 0.4mm pitch between the top and bottom PoP package. Test vehicle has 0.1mm thick TSV substrate and bare-die flip-chip, achieving 0.7mm total stackup height vs. equivalent organic PoP of ~1.5mm.

This paper will highlight the TSV interposer test vehicle design, fabrication, assembly process development, warpage behavior study with simulation and experimentals, component level reliability test results of the Super Thin PoP test vehicle and future steps.

1. Introduction

Increasing demand for new and more advanced electronic products with a smaller form factor, superior functionality and performance with a lower overall cost has driven semiconductor industry to develop more innovative and emerging advanced packaging technologies.

One of the hottest topics in the semiconductor industry today is a 3D packaging using Through Silicon Via (TSV) technology. Driven by the need for improved electrical performance or the reduction of timing delays, methods to use short vertical interconnects have been developed to replace the long interconnects found in 2D packaging. The industry is gearing up to move from technology path finding phase for TSV into commercialization phase, where economic realities will determine the technologies that can be adopted. Choosing the right process equipment and materials with innovative design solutions addressing thermal and electrical issues will be the key success factor.

3D integration is progressing on three fronts starting with package-level (die, package stacking), wafer level (die-to-wafer bonding, fan out WLP) and more recently at the Si level (TSV) as shown in Figure 1 [1].

![Figure 1. 3D Integration- The solution space – 3D @ package level, wafer level & Si level](image)

Gaining in popularity for many reasons, 3D TSV interposers are not considered as a just temporary measure or stepping-stone technology anymore. The consensus is that interposers may act as a bridge to full 3D IC integration in some applications, but they also remain a viable enabling technology for new applications requiring high-density 3D package integration architectures.

3D TSV interposer is an efficient and practical approach to solving die integration challenges. Many microsystem devices that will have to move to wafer-level packages will also facilitate further integration using silicon TSV interposers [2].

2. Super Thin TSV PoP Project Overview

This paper will focus on the development of the Super Thin TSV PoP Package including the following aspects:

- The design of the TSV substrate and PoP test vehicles
- TSV interposer fabrication and process development
- TSV assembly process development and characterization
- Component level and board level reliability characterization


The test vehicle consists of two very thin PoPs. The bottom PoP is representative of an advanced flip chip PoP (fcPoP) for logic processor device in production today with respect to its size and ball count (12x12mm and 547 balls at 0.4mm pitch), but utilizing an Si based substrate of 0.10mm thickness instead of conventional organic substrate thickness.
of over 0.30mm. The top PoP is meant to represent a future memory device that would be stacked on such a logic processor in advanced mobile phones. This top PoP also utilizes the 0.10mm thick Si based substrate and has a flip chip memory device mounted on the top surface. Only one such memory device is attached for this initial study. More than one memory device could be stacked utilizing TSV stacking of memory in the future. This top PoP is also 12x12mm size with 216 balls at 0.4mm pitch. Figure 1 shows the details of the PoP test vehicles after they are stacked together. Top package has peripheral 2 row balls (168 I/O) for bottom package interconnection as shown in Figure 2 while bottom package has full array structure with minor depopulation (547 I/O). The overall thickness of 0.7mm max is much thinner than anything on the market today due to the utilization of the thin TSV substrates and the 0.4mm ball pitch on both PoPs.

In order to perform subsequent reliability tests and board level reliability (BLR), each PoP was made a daisy chain (DC) package with the DC going through both the package TSV substrate and also through the flip chip die mounted to each PoP. The DC scheme is such that after the PoPs are stacked that each net can be monitored independently. Of course this is very useful when performing the BLR as each net can have its own channel on the event detector (ED) used to monitor the test, thus the net or chain that is failing in the PoP stack can be easily determined during the BLR drop test or temperature cycle on board (TCoB).

![Figure 1. Super Thin TSV PoP test vehicle](image)

Hence, there are four nets that can be accessed from the bottom of the bottom PoP and monitored after the PoP is stacked on the board using the ED.

For the bottom PoP the three corner balls in each corner are excluded, but they are tied into a separate net that can be monitored on the test board without ED. For the top PoP, one ball at each corner is excluded, but also can be monitored on the test board without ED.

Another feature built into the TSV substrate for the top and bottom PoP is that half of the balls have TSV in ball pad whereas the other half has TSV off ball pad. The net is continuous through all of these balls but the thinking is that failure analysis (FA) can be done later to determine if there is any difference in reliability between the two ball pad types.

![Figure 2. TSV PoP specification](image)

![Figure 3. Test vehicle bump structure](image)

The bump structure and composition for the test vehicles can be seen in figure 3. 0.04/0.08mm bump pitch was implemented at the periphery of the logic flip chip DC. Option 2 structure in Figure 3 showed less warpage during flip chip reflow and was used in this initial development.

4. Fabrication and Assembly of Super Thin TSV PoP

The basic process flow is shown in figure 4. 200mm wafers were used to make both the TSV substrates and the flip chip TV DC dice to be mounted on each PoP substrate. A via first process was used to make the TSV. The TSV is 0.050mm in diameter and targeted 0.105mm deep using DRIE (Deep Reactive Ion Etching) process. PECVD (Plasma Enhanced Chemical Vapor Deposition) was used to make over 200nm conformal silicon oxide isolation at via wall. PVD (Physical Vapor Deposition) was used to make Ti/Cu layer prior to filling with Cu using electro-plating. No voids were observed and annealing was done for stress relaxation with Cu recrystalization as used in Cu damascene process. The wafer is thinned to reveal the Cu TSV followed by CMP.
(Chemical Mechanical Polishing), RDL, and UBM for ball and bump pads on one side. Temporary bonding to a handler wafer is used to enable thinning of the TSV wafer and processing of the RDL and UBM. Solder printing and reflow is used to cover the bump pads and top land pads on the TSV substrate. A chip-to-wafer (CtW) approach was used to attach the flip chip DC die to each TSV substrate unit in wafer form, followed by underfill process as shown in figure 6&7. The TSV wafer with chip mounted and underfilled is then debonded from the handler wafer, flipped and bonded to another handler on the chip attached side to enable solder ball attach on the bottom side of the TSV substrate. The package is now saw singulated and deboned. The individual TSV PoPs are now ready for testing and pick and place for stacking onto PCBs as shown in figure 8.

Many processes were developed and characterized in order to yield good units. A lot of work focused on the TSV process as well as thinning and handling of wafers, especially bonding and debonding without mechanical damage and residue or contamination.

Figure 4. Overall process flow: TSV fabrication and packaging process

Figure 5. TSV interposer fabrication process flow

Figure 6. Flip chip to substrate interconnect

Figure 7. Chip-to-wafer bonding

Figure 8. Photos of TSV super thin PoP packages: bottom (left) and top (right) packages

Figure 9. SEM micrograph of cross-section of super thin TSV PoP: (a) overall PoP and (b) enlarged of solder ball interconnects between top and bottom packages
5. Warpage Behavior of TSV super thin PoP

Among the 3D technologies, Package-on-Package (PoP) is increasingly becoming mainstream due to its flexibility of combination and sourcing. The top package to be stacked using solder ball interconnects. For successful package on package stacking with high assembly yield, warpage of both the top and the bottom package are critical. If the warpage is too large, open solder joints may occur between the bottom package and motherboard, or between the bottom package and top package. Not only is the warpage at room temperature a concern for co-planarity measurement as a control, but warpage at solder reflow temperatures (up to 260°C for lead-free solder) should also be considered since open solder joints occur during solder solidification. As a result, warpage control at both temperature extremes is critical for 3D PoP stacking.

Warpage had to be carefully optimized and controlled to realize high chip attach yields given the 80/40um bump pitch devices. A key attribute and goal of the Super Thin TSV PoP was to realize a thinner PoP by using the 0.10mm Si substrate and also thinner warpage during reflow temp by using Si substrate. As shown in figure 10, thermo-mechanical simulation was carried out with conditions of:

- Assumptions: Stress free at underfill curing temperature, no UF shrinkage, metal layer of die (<5% in volume fraction) ignored
- 2 interposer structure, 2 FC-die thickness, and 3 UF materials simulated

Table 1 shows DOE study of warpage behavior as function of silicon substrate design (core and dielectrics thickness), die thickness and underfill material. Thin flipchip die shows more warpage and thicker core with thinner dielectrics layer shows also more warpage.

The design of (2)-A in Table 1 (68um core/75um die/UF-A) was selected for test vehicle in this study. Simulation data showed 32.4um(at RT), 10.3um (at 260°C) and measured warpage was 25um (at RT) and 15um (at 260°C). So simulation results was in good agreement of actual warpage data.

Figure 11 shows Thermo-Moire warpage data less than 30um at reflow temperatures for the bottom TSV PoP which is within the warpage tolerance allowance for 0.4mm package interface pitch target [4]. In comparison with conventional flipchip-PoP-bottom package of 12x12mm, super thin PoP bottom packages showed much less warpage over reflow temperature profile range.

Table 1. Summary of DOE study of warpage simulation

<table>
<thead>
<tr>
<th>Silicon substrate design</th>
<th>Die Thick (um)</th>
<th>Underfill Material</th>
<th>Warpage @ 25°C</th>
<th>Warpage @ 200°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) 76 μm core 4.5 μm passivation</td>
<td>75</td>
<td>A</td>
<td>38.5</td>
<td>5.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B</td>
<td>32.6</td>
<td>4.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C</td>
<td>26.5</td>
<td>4.9</td>
</tr>
<tr>
<td>(2) 68 μm core 6.5 μm passivation</td>
<td>75</td>
<td>A</td>
<td>32.4</td>
<td>10.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B</td>
<td>29.0</td>
<td>9.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C</td>
<td>26.0</td>
<td>8.7</td>
</tr>
<tr>
<td>(3) 68 μm core 6.5 μm passivation</td>
<td>100</td>
<td>A</td>
<td>20.9</td>
<td>11.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B</td>
<td>27.7</td>
<td>10.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C</td>
<td>20.5</td>
<td>11.2</td>
</tr>
</tbody>
</table>

6. Component Level Reliability Test

TSV super thin PoP packages, top and bottom, both were sent to JEDEC standard reliability tests. For each test
conditions, 77 samples were prepared. Using test socket designed for electrical connectivity as shown in figure 13, all test samples were electrically measured its connectivity before and after reliability tests. Reliability samples passed MSL-3 with 3x reflow process at Pb-free 260°C peak temperature. All samples passed unbiased HAST and HTS reliability tests. There was no failure found after 1000 cycle T/C and 1000 hr HST.

![Figure 13. Test socket for electrical testing of super thin PoP packages](image)

Table 2. Super Thin PoP component level reliability test results.

<table>
<thead>
<tr>
<th>Rel Test</th>
<th>Conditions</th>
<th>JEDEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preconditioning</td>
<td>Pre-determine during</td>
<td>J-STD-020</td>
</tr>
<tr>
<td></td>
<td>Package Qualification</td>
<td>JESD22-A113</td>
</tr>
<tr>
<td>HAST (Unbiased)</td>
<td>130°C, 85% RH (96hrs)</td>
<td>JESD22-A118</td>
</tr>
<tr>
<td>Temp Cycling (TC)</td>
<td>-55°C/125°C (1000x)</td>
<td>JESD22-A104</td>
</tr>
<tr>
<td>High Temp Storage (HTS)</td>
<td>150°C (1000hrs)</td>
<td>JESD22-A103</td>
</tr>
</tbody>
</table>

7. Future Work
Future work is already underway to do board level reliability (drop test and TCoB).

8. Conclusions
A novel very thin PoP solution utilizing a thin TSV substrate instead of conventional multi-layer organic substrates. The DC TV was designed in order to enable testing and BLR of each element of the structure. Warpage simulation was carried out to investigate silicon substrate design, die thickness and underfill material for overall package warpage. And Thermo-Moire warpage measurement was performed for test samples. Super Thin PoP showed 30um warpage along reflow profile range and it has much less warpage than conventional flipchip PoP bottom. The TSV and assembly process were developed in order to realize good packages that are now ready for board level reliability. Super thin PoP passed successfully JEDEC standard component level tests. The goal of showing the viability or producing thinner and lower warpage PoP packages by utilizing TSV substrates was realized.

Acknowledgments
The authors would like to acknowledge the work of Mr. Chow Seng Guan of STATS ChipPAC, Inc. for thermo-mechanical warpage simulation. Also would like to thank Il Kwon Shim and the Wafer Integration Team at STATS ChipPAC R&D in Singapore.

References