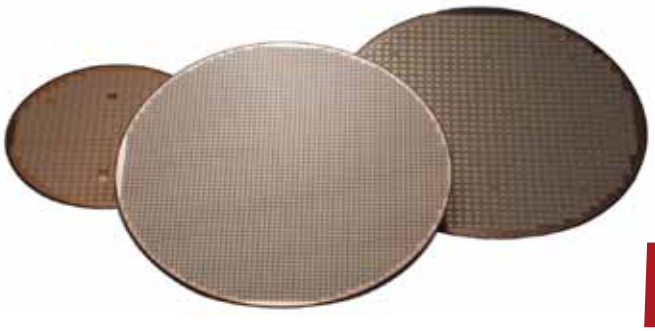


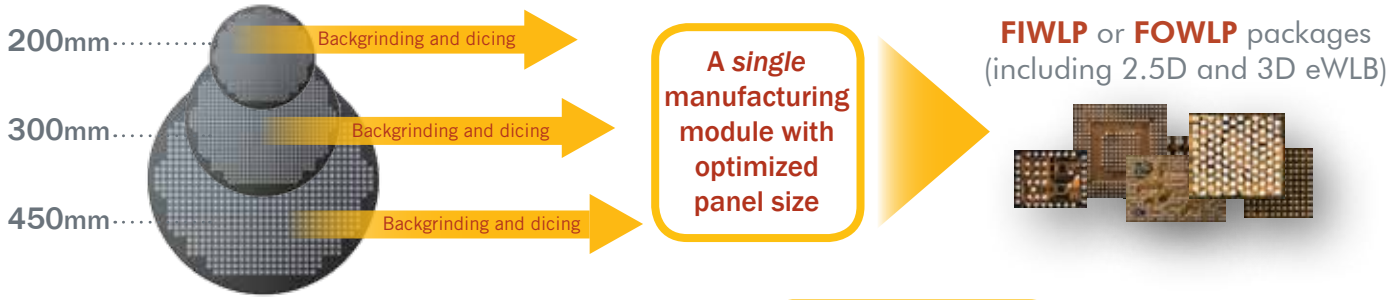
Innovations in Wafer Level Technology

A proven leader in Wafer Level Packaging technology

The demand for breakthrough performance in cost effective solutions has driven integration technology to new levels of complexity in semiconductor package designs. The mobile market is accelerating demand for more compact and complex semiconductor packages that are challenging traditional packaging technology in the areas of form factor, reliability and performance, and integration is increasingly moving from substrate-based package configurations to more complex wafer level package designs.

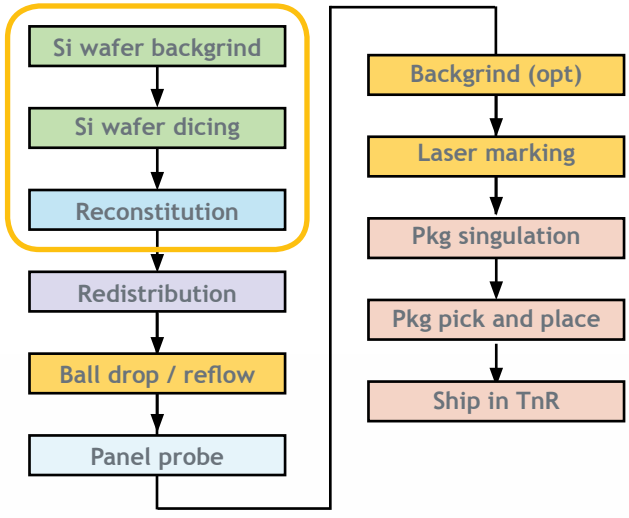
As die sizes and lithography nodes shrink, STATS ChipPAC is actively pushing the boundaries of traditional paradigms by pioneering a number of enabling integration technologies in wafer level packaging. STATS ChipPAC is an industry leader in providing a comprehensive platform of advanced wafer level solutions including Fan-out Wafer Level Packaging (FOWLP), Fan-in Wafer Level Packaging (FIWLP), Through Silicon Via (TSV) and Integrated Passive Devices (IPD) for mobile handsets, smartphones, tablets and wearable devices.

A new paradigm in Wafer Level manufacturing: FlexLine™



FlexLine™ is an innovative manufacturing approach that provides freedom from wafer diameter constraints, while enabling supply chain simplification and significant cost reductions not possible with a conventional manufacturing flow. This breakthrough approach delivers unprecedented flexibility in producing **both fan-out wafer level packages (FOWLP) and fan-in wafer level chip scale packages (WLCSP)** on the same manufacturing line.

The FlexLine™ method is based on the advanced manufacturing process for FOWLP technology known as **embedded Wafer Level Ball Grid Array (eWLB)**. What is unique to the eWLB manufacturing process is the wafer reconstitution step where the incoming wafers are diced at the start of the process and then the die are reconstituted into a uniform wafer or panel size.



The FlexLine™ process flow leverages the eWLB Fan-Out package process

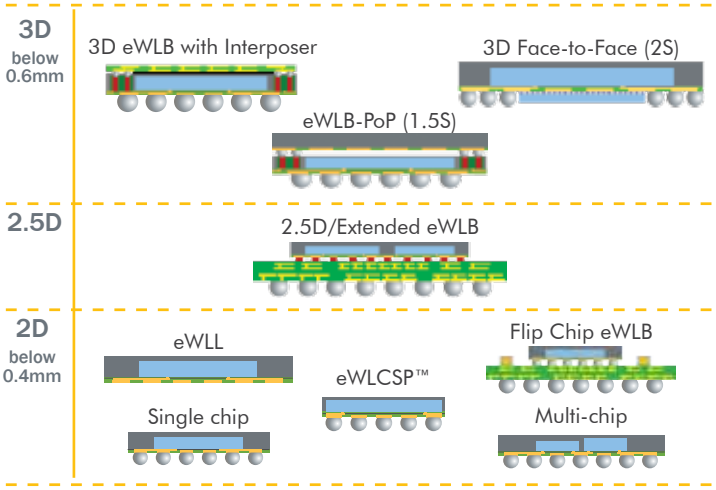
Leveraging the Fan-Out manufacturing process

By normalizing incoming wafer diameters to a uniform processing size, the original wafer diameter no longer dictates manufacturing or process capabilities. The FlexLine method can seamlessly process any incoming silicon diameter without a change in equipment set or bill of materials used in the packaging process.

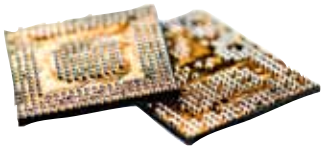
Now one qualified manufacturing source can provide FIWLP and FOWLP, including 2.5D and 3D eWLB, using the same equipment, device structures, material sets and location. And, as the FlexLine™ panel size increases, it effectively lowers the overhead processing cost per unit, and provides semiconductor customers with a cost effective solution for current and future wafer level technologies.

The FlexLine™ process has been qualified at advanced silicon nodes down to 28nm, ball pitches down to 0.40mm and body sizes as small as 2.5x2.5mm.

The FlexLine™ advantage is available in a wide range of wafer level packages.



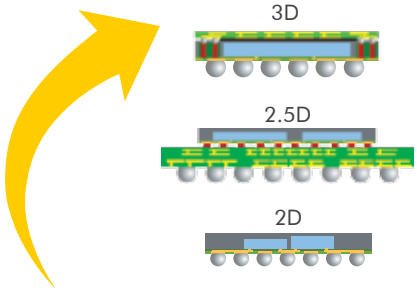
A new path for 3D integration: embedded Wafer Level BGA (eWLB)



eWLB is a versatile platform for 2D, 2.5D and 3D integration that delivers significant product advantages in terms of higher input/output (I/O) and thinner profiles in a reliable, cost effective package. A powerful FOWLP technology, eWLB has the design flexibility to accommodate an unlimited number of interconnects and is unconstrained by die size. This enables eWLB to deliver maximium connection density, improved electrical and thermal performance and smaller package dimensions to meet the relentless form factor and performance requirements of the mobile market, and is now the preferred packaging solution in smartphones, tablets and wearable devices.

One of the first companies to ramp eWLB to high volume production, STATS ChipPAC is an industry leader in eWLB technology, providing innovative package designs and an efficient manufacturing process that is well-suited for a multitude of complex and highly integrated solutions including 2.5D and 3D integration, including Si partitioning.

STATS ChipPAC's 2.5D and 3D solutions offer more cost effective and infrastructure-friendly alternatives to TSVs by achieving tighter line/spaces for a range of configurations that deliver product advantages to customers in terms of higher performance, higher frequencies, higher bandwidth and thinner package profiles.

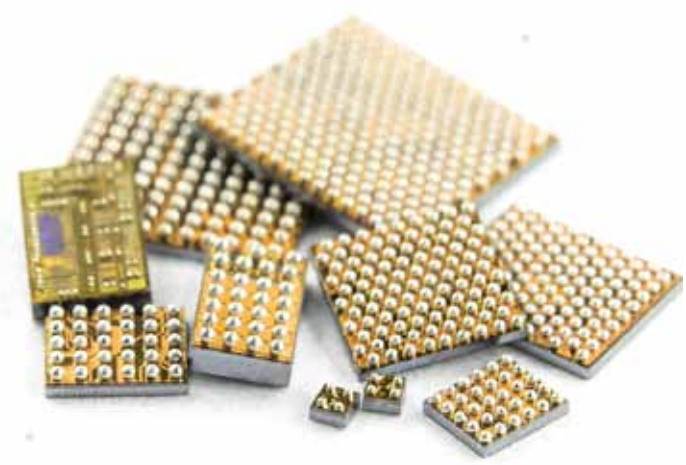


Unique multi-die 2.5/3D integration with a quantum leap in density and form factor

STATS ChipPAC offers the most comprehensive Fan-Out portfolio in the industry:

- Wide range of small die, large die, flip chip, stacked or side-by-side multi-die and ultra-thin options
- Body sizes: 2.2 x 2.2mm – 14 x 14mm and expanding (package size dependent on die size)
- 2.5D eWLB interposer solutions (replaces stacked package configurations or to enable 3D TSV)
- 3D System-in-Package (SiP) and Package-on-Package (PoP) solutions include multiple embedded passives and active components, face-to-back or face-to-face options, and single-sided, 1.5-sided and double-sided PoP configurations (total stacked PoP height <1.0mm)

Fan-In WLP: Wafer Level Chip Scale Packages (WLCSP)



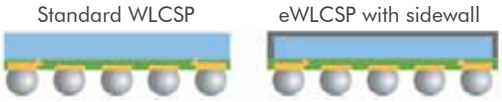
As a small, lightweight, high performance semiconductor solution, **WLCSP is a FIWLP technology that offers compelling packaging solutions for cost and space constrained mobile devices and new applications such as wearable technology.** WLCSP is a true Chip Scale Packaging (CSP) technology where the package is the same size as the die, and the cost per package is primarily determined by the number of die per wafer rather than the number of I/O per device.

STATS ChipPAC offers high performance WLCSP solutions that provide significant package footprint reductions, lower cost, improved electrical performance, and a relatively simpler construction over conventional wirebond or interposer packaging technologies.

The FlexLine advantage: encapsulated WLCSP (eWLCSP™)

Utiliziing the FlexLine™ manufacturing approach, STATS ChipPAC has developed an innovative packaging technology called **encapsulated Wafer Level Chip Scale Package (eWLCSP™)**. eWLCSP™ offers significant structural advantages over traditional WLCSP designs. As a bare die package, WLCSP is regularly exposed to potential cracking, chipping and handling issues that can occur before or during the SMT assembly process. This is particularly true for advanced node products where the die is very thin and dielectric layers are extremely fragile.

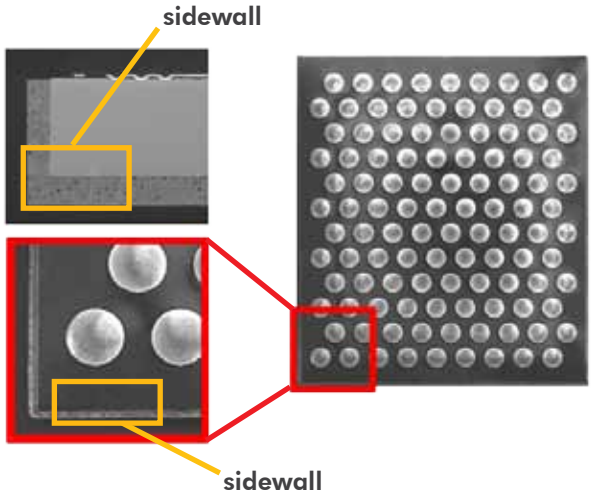
eWLCSP™ is equivalent to a conventional WLCSP product with the addition of a thin protective coating on the backside and four sidewalls of the die, achieving increased durability and reliability within the standard WLCSP size specification.



Encapsulation offers a variety of advantages:

- Light and mechanical protection
- Alleviates die chipping
- Enables more effective positioning on the printed circuit board (PCB)
- Protects the silicon during socket insertion for test

In addition, eWLCSP electrical performance is equivalent to WLCSP with proven results in component level reliability (CLR), temperature cycle on board (TCoB) and drop test.



Encapsulation offers sidewall protection

FlexLine™ eWLCSP Cost Reductions

A product currently using a conventional WLCSP process can be converted to eWLCSP without any silicon design change required, regardless of the current silicon wafer diameter. The FlexLine method can reduce WLCSP costs by 15-30% when using the optimum design requirements for WLCSP devices. For example, using the FlexLine method, 200mm incoming wafers can be reconstituted into 300mm or larger panel sizes, providing customers with the advantage of panel size scaling--with further per-unit cost reductions as panel sizes increase.

Integrated Passive Devices (IPD)

Passive devices such as resistors, capacitors, inductors, filters and baluns can consume 60-70% of available space in a system, subsystem or System-in-Package (SiP). One of the first companies in the industry to integrate and fabricate passive devices at the silicon wafer level, STATS ChipPAC is able to produce IPDs which are significantly smaller, thinner and higher performing than standard discrete passive devices that are commercially available today. With this knowledge and experience, STATS ChipPAC has been able to embed passive devices in very close proximity to the active die, providing significant performance, size reduction and device integration in System-in-Package (SiP) configurations that address 2.5D and 3D integration requirements.

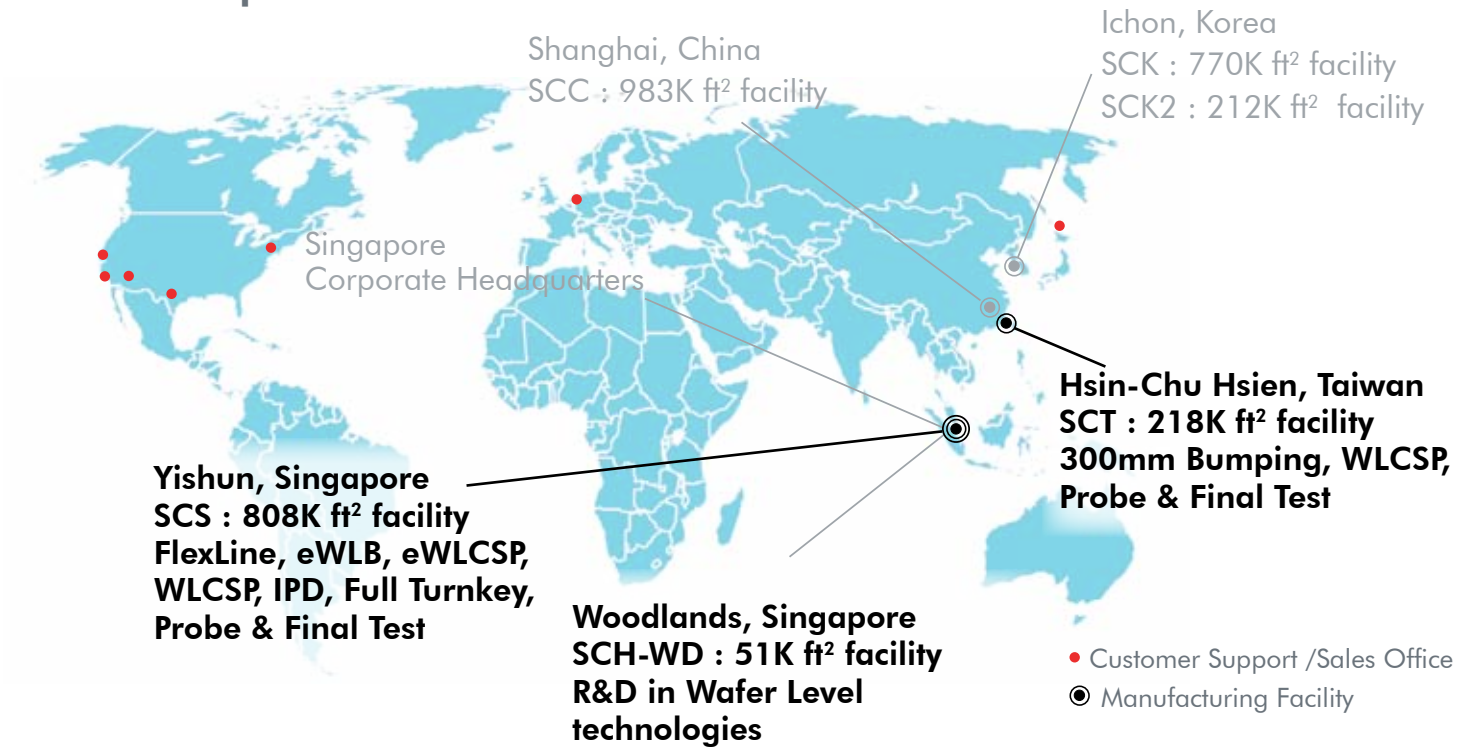
Through Silicon Vias (TSV)

STATS ChipPAC was one of the first OSAT providers to invest in **back-end of line (BEOL)** manufacturing capabilities for 2.5D and 3D TSV technology. STATS ChipPAC's BEOL services include chip-to-chip and chip-to-wafer assembly with stealth dicing and fine pitch micro-bump bonding down to 40um.

STATS ChipPAC's TSV capabilities also include 300mm **mid-end of line (MEOL)** processing capabilities in areas such as TSV formation and metallization, bumped wafer thinning, thin wafer handling, 3D microbump bonding, wafer-level underfill and TSV assembly.

To provide a "bridge" between today's 2D packaging solutions and next-generation 3D technology, STATS ChipPAC also offers **TSV interposer processing and assembly**. TSV interposers provide flexibility for the integration of die from different technology nodes and deliver advantages in miniaturization, thermal performance and fine line/width spacing in a semiconductor package.

STATS ChipPAC's WLP centers of excellence



To find out more about STATS ChipPAC's Wafer Level technology offering, visit us online at www.statschippac.com

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