

System-in-Package (SiP) Solutions



Semiconductor companies are continually faced with complex integration challenges as consumers want their electronics to be smaller, faster and higher performance with more and more functionality packed into a single device. This demand for miniaturization and modularization of

functionality in a single package combined with the increasing cost per transistor of advanced Silicon nodes beyond 28nm is rapidly moving the microelectronics industry toward system level integration.

Advanced packaging has a significant impact on addressing these challenges. Semiconductor companies are increasingly looking to their outsourcing partners to provide highly integrated advanced packaging solutions for their end products. System-in-Package is a high performance solution that can meet the current and future demands for greater system performance, increased functionality, reduced power consumption and reduced form factor in a wide range of markets and applications.

SiP is a functional electronic system or sub-system that includes two or more heterogeneous semiconductor die (often from different technology nodes optimized for their individual functionalities), usually with passive components.



>1 Die
+ Passives
+ Others



Advantages of SiP

To meet the need for increased integration, improved electrical performance, reduced power consumption, faster speed and smaller device sizes, several advantages are driving the industry towards SiP solutions including:

- » Thinner / smaller form factor than individually packaged components
- » Increased performance and functional integration
- » Design flexibilities
- » Better electromagnetic interference (EMI) isolation
- » Reduced system board space and complexity
- » Improved power management and more room for battery
- » Simplified SMT assembly process
- » Cost effective "plug-and-play" solutions
- » Faster time-to-market (TTM)
- » One stop turnkey solution - Wafer to fully tested SiP modules



With these advantages, SiP is able to address some of the limitations of silicon (Si) level integration (commonly known as System-on-Chip or SoC), including design complexities, long development cycles, manufacturability, intellectual property (IP) and legal issues, longer time-to-market and higher costs. SiP provides a high performance packaging solution that is scalable, cost effective and can be easily implemented in an electronic device.

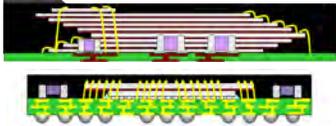
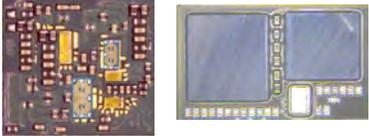
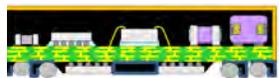
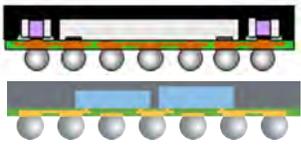
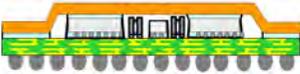
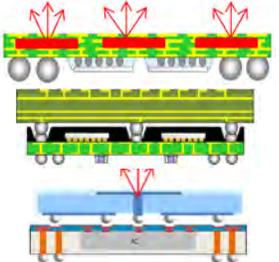
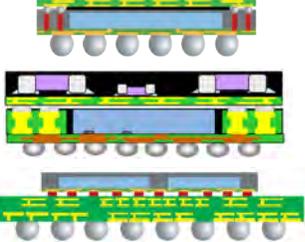


Comprehensive Capabilities for SiP Markets and Applications

We have a comprehensive SiP portfolio to serve multiple markets and end applications. Today, SiP and miniaturized modules are being utilized in a number of markets such as mobile devices, Internet of Things (IoT), wearables, healthcare, industrial, automotive, computing and communication networks. Each SiP solution varies in complexity based on the

number and functionality of the components required by each application.

Below are some examples of our SiP solutions and end-market applications.

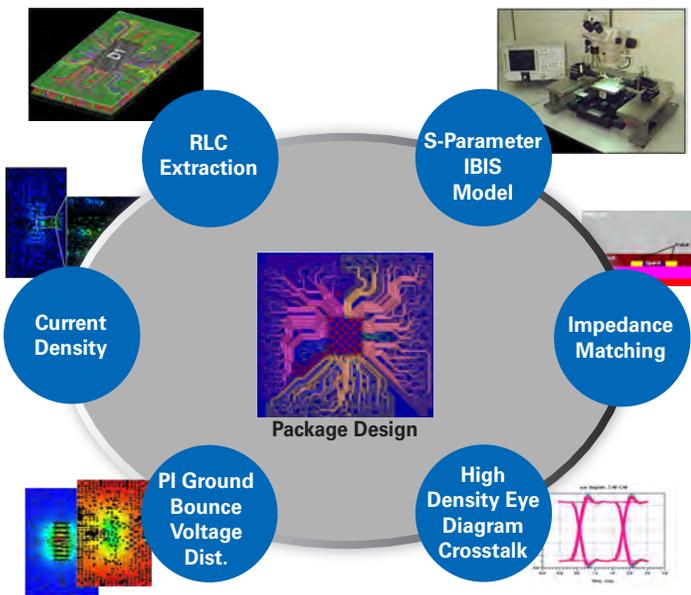
SiP Package Configurations	Examples	Features	Target Applications
Stacked Die Module		<ul style="list-style-type: none"> LGA/BGA Thin/stacked die Passives 	<ul style="list-style-type: none"> SSD (removable & embedded) Baseband / application processor (Wearables)
Substrate Module		<ul style="list-style-type: none"> LGA/BGA Bare die or over mold IPD, passives 	<ul style="list-style-type: none"> Filters Power amplifier (PA) modules Connectivity combo modules
fcFBGA/LGA SiP		<ul style="list-style-type: none"> Passives, WLCSP, packaged components Coreless or cored substrates 	<ul style="list-style-type: none"> Controller modules Power amplifier/ Power amplifier duplexer modules RF Front-end modules (FEM)
Hybrid (flip chip + wirebond) SiP - single sided			
Hybrid SiP - double sided		<ul style="list-style-type: none"> Double sided assembly with active and passives Coreless or cored substrates 	<ul style="list-style-type: none"> RF Front-end modules (FEM) Connectivity combo modules
eWLB SiP		<ul style="list-style-type: none"> Multi die Embedded passives 	<ul style="list-style-type: none"> Connectivity PMIC, CODEC Power amplifier modules Application processor + memory RF MEMS
fcBGA SiP		<ul style="list-style-type: none"> Multi die Packaged and bare die DRAM and passives Advanced thermal management Large body 	<ul style="list-style-type: none"> CPU/GPU + memory Networking, gaming Automotive
Antenna-in-Package - SiP Laminate eWLB		<ul style="list-style-type: none"> Embedded or discrete antenna PoP antenna Fan-out or laminate base Low loss materials 	<ul style="list-style-type: none"> 5G communication Automotive radar, LIDAR
eWLB-PoP & 2.5D SiP		<ul style="list-style-type: none"> eWLB-PoP Fine pitch and high I/O 	<ul style="list-style-type: none"> High-end application processors CPU/GPU High bandwidth

Design, Assembly and Test Capabilities

Design and Simulation

In the drive for system miniaturization, semiconductor companies face complex issues in developing highly integrated package designs. Our experienced R&D and engineering teams are here to support customers faced with complex SiP integration requirements. Our capabilities and services in SiP module design are supported by advanced electrical, mechanical and thermal simulation.

Typical Design and Simulation Flow



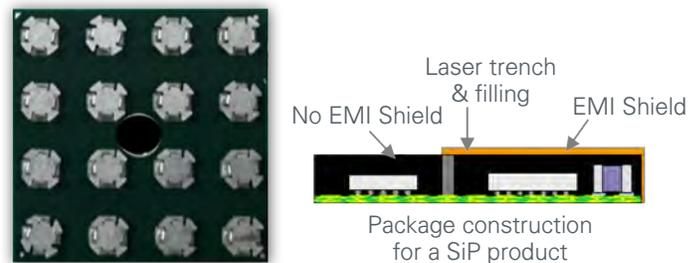
Our Surface Mount Technology (SMT) design rules are being advanced through refinements in materials and process technologies to enable tighter component-to-component placement, and molding technologies and compounds are being improved to enable lower mold cap profiles and smaller dimensions. We work with advanced substrate materials with fine line width/spacing (L/S), reduced dielectric thickness, and coreless design to address the reduced form factor requirements of next generation applications while enabling a lower cost.

Vertical integration brings about higher component density and optimizes the board space needed in the end device, allowing for a larger battery space or smaller overall size. Our expertise in embedded wafer level ball grid array (eWLB) using advanced L/S and via density design rules, with the cost effective integration of passives and multiple embedded die in advanced eWLB SiP configurations offers further form factor reduction and lower package profiles.

Assembly

SiP solutions require multiple packaging technologies such as fine pitch flip chip, wire bonding, wafer level packaging (WLP) and eWLB, IPDs and embedded die to meet the specific requirements for a product. The specific technology used in each application varies in complexity based on the number and type of components as defined by the application and cost requirements. In addition to the packaging technology, there are important technical requirements for an SiP solution, including advanced substrates, high density surface mount technology (SMT) placement, enhanced molding processes, and electromagnetic interference (EMI) shielding.

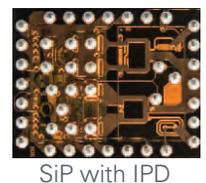
EMI shielding has become essential for applications such as RF/mobile and connectivity SiPs. As operating frequencies increase and devices become more complex, electronic devices are more susceptible to electromagnetic interference (EMI). EMI shields can prevent interference from either a device generating interference out to the world or the device picking interference from outside sources into itself.



SiP provides the ability to partition different segments of the system functionality while EMI shielding protects different circuit segments from EMI interferences and noise susceptibility. We can offer a portfolio of shielding options, including fully automated in line conformal shielding, compartmental and selective shielding to serve the diverse needs of current and next generation RF/mobile and connectivity SiPs.

Our manufacturing capabilities such as advanced SMT with high accuracy component placement, advanced molding for complex SiP typography applications, EMI conformal shielding and high process yields, coupled with our high volume SMT line and fully automated loading/unloading process in the EMI shielding process, ensure that our customers receive fast, high quality, cost effective solutions.

As one of the first companies in the industry to integrate and fabricate passive devices at the Si level, we are able to produce IPDs which are significantly smaller, thinner and higher performing than standard discrete passive devices and embed them in very close proximity to the active die, providing significant performance, size reduction and device integration in SiP configurations.



Test Services

To meet the need for increased integration, improved electrical performance, reduced power consumption, faster speed and smaller device sizes, several advantages are driving the industry towards SiP solutions including:

- » Experience in RF ATE production on Advantest RF (< 6 GHz), Teradyne RF system (< 6GHz), LTX-CX (< 6 GHz) and NI-PXI (<6 GH) platform
- » Capability on FE12/FE24 RF option for PS800/PS1600 (Advantest RF)
- » Capability on Microwave option (GEN4/UltraWave12G) for Catalyst/IFLEX/uFLEX (Teradyne RF)
- » Experience in RF mass production volume test and multiple sites (up to 16 sites and 600Munits over last 5 years)
- » Proven RF Test Development Engineering on 60GHz Transceiver, GPS, RFFE Envelope Tracker, etc.

cost reduction, performance enhancements, and faster time-to-market for innovative solutions in the mobile, IoT, wearables, automotive, computing and other market segments.

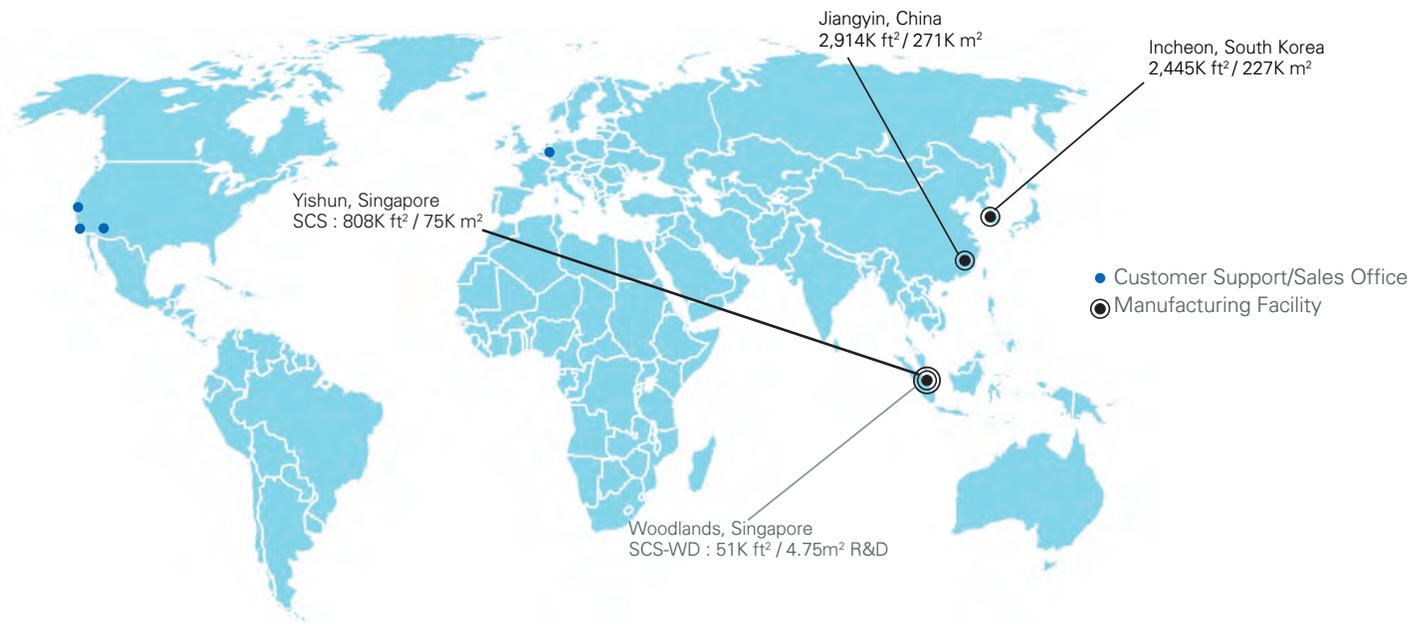
As demand for complex, highly integrated electronics devices continues to grow and evolve in the semiconductor industry, you can rely on our advanced technology and manufacturing experience to deliver the optimum SiP solution for your competitive integration needs.



Full Turnkey Solutions

Altogether, our advanced capabilities, from design to assembly and test, along with our flexible business model, high throughput and high yield automated processes, have enabled us to serve our customers worldwide to achieve higher integration, miniaturization,

Manufacturing Operations



To find out more about our SiP solutions,
visit us online at www.statschippac.com or www.jcetglobal.com.

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