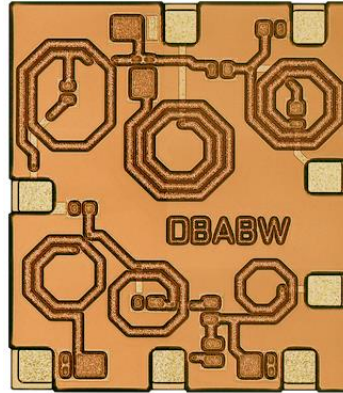


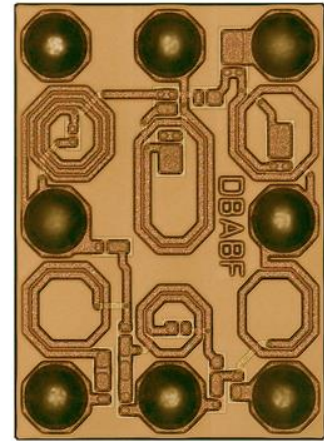
(29) WLAN Diplexer (SCI-503W/F)

FEATURES

- Passive integration on silicon substrate
- Low insertion loss in pass band
- Small size: 1.4 mm x 1.2 mm (wirebond)
1.6 mm x 1.2 mm (flip chip)
- Eutectic Sn/Pb or lead-free solder bump
- Low profile, 0.40 mm height
- Directly attachable on PCB or flipped on PCB
- Operating temperature: -40 to +85 °C
- Storage temperature: -40 to +85 °C



SCI-503W (Wirebond)



SCI-503F (Flip Chip)

DESCRIPTION

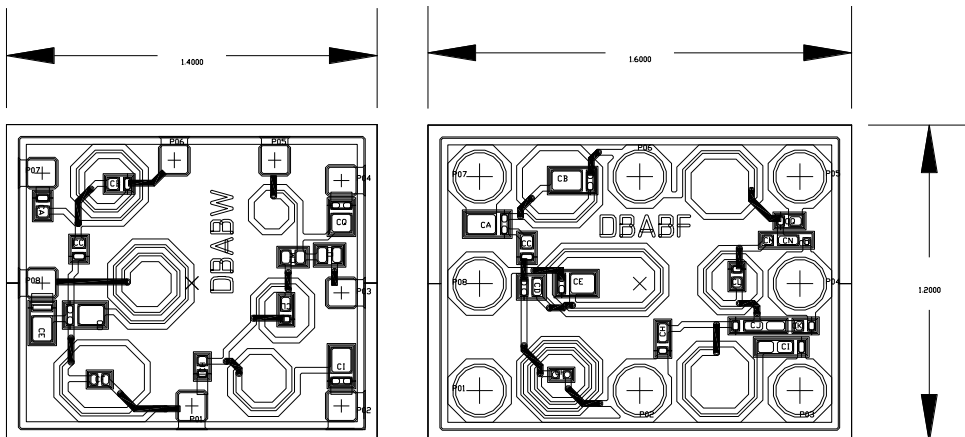
STATS ChipPAC's SCI-503W/F is a diplexer for WiFi band applications. The diplexer has low pass-band insertion loss and small size. It is composed of 8.0 μ m Cu-plated inductors and Metal-Insulator-Metal capacitors which are fabricated on a silicon substrate using our IPD (Integrated Passive Device) process. The pad or bump size and pitch of the diplexer are selected so that the device can be mounted directly on a PCB or laminate substrate using conventional wirebonding or surface mount techniques. The low profile and small form-factor of the device make it especially suitable for SiP applications.

ELECTRICAL SPECIFICATIONS

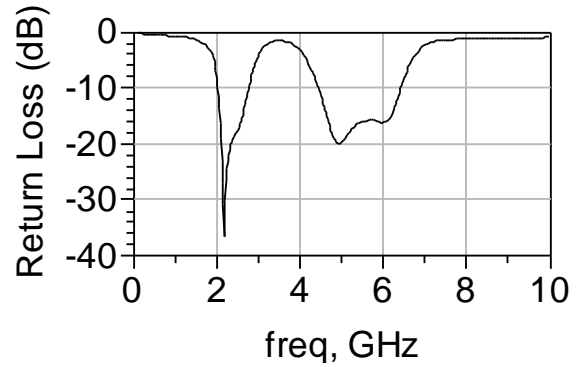
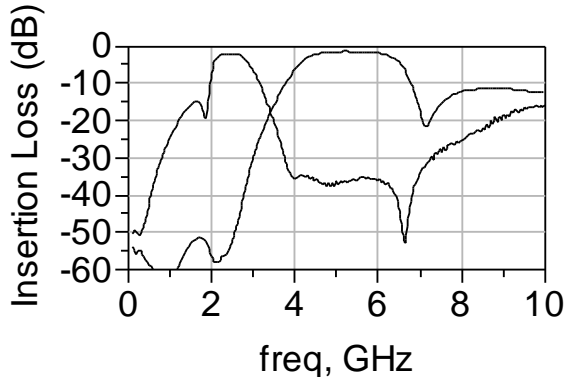
(Test board loss 0.1 dB and 0.25 dB included)

Specification	Unit	Minimum	Typical	Maximum
Pass Band 1	MHz	2400		2500
Pass Band 2	MHz	5115		5825
Insertion Loss, Band 1	dB		2.1	
Insertion Loss, Band 2	dB		1.9	
Return Loss, Band 1	dB		15	
Return Loss, Band 2	dB		15	
Isolation, Band 1 at Band 2	dB		35	
Isolation, DC-1.7 GHz	dB	15		
Isolation, Band 2 at Band 1	dB		50	
Isolation, 6.9-10.0 GHz	dB	12		
Size	mm	1.4 x 1.2 (WB)		1.6 x 1.2 (FC)

DIMENSIONS

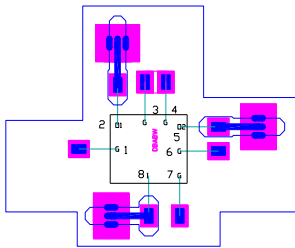


TYPICAL CHARACTERISTICS

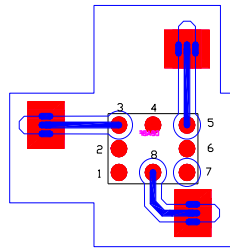


TEST BOARD DRAWING

SCI-503W (Wirebond)



SCI-503F (Flip Chip)



Pad	SCI-503W Signal	SCI-503F Signal
1	GND	GND
2	2G Output	GND
3	GND	5G Output
4	GND	GND
5	5G Output	2G Output
6	GND	GND
7	GND	GND
8	Common Input	Common Input

NOTES

All dimension measurement units are in millimeters (mm). Electrical performance and typical values are measured at room temperature. For best results, ground plane directly beneath the device should be in the top metal layer.

Refer to "Appendix A" for:

- Pad sizes and typical wirebond length used in the wirebonded IPD products.
- Recommended solder thermal profile, landing pattern recommendation and bump specifications used in the flip chip IPD products.