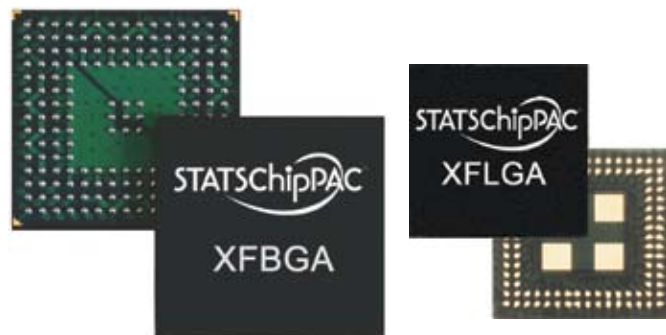


Extremely Thin Profile Array Packages

XFBGA, XFLGA, X1FLGA

- Extremely thin packaging solutions
- Profile heights less than 0.50mm
- Advanced molding technology
- Extra thin design allows full array of solder balls (BGA) or lands (LGA)
- Available in single or multiple die solutions



FEATURES

- Profile heights less than 0.5mm
- 0.25mm mold cap
- 75µm die thickness
- 0.13mm substrate thickness (2 metal layer laminate substrate)
- Flexible body sizes ranging from 4 x 4mm to 15 x 15mm
- 0.80, 0.65 and 0.50mm ball pitch
- 50µm solder bumping on substrate
- Utilizes conventional wire bond equipment and processes
- Wide range of custom and open tool designs available
- Pb-free material set options (including low alpha materials)
- JEDEC standard compliant

APPLICATIONS

- Space constrained portable electronics such as cell phones, mini disk drives, and miniaturized consumer electronics
- Memory cards and USB drives
- Stacked packages

DESCRIPTION

Space constrained portable electronics such as cell phones, mini disk drives, and miniaturized consumer electronics are driving the need for smaller and thinner packaging solutions to support low vertical profiles.

By combining conventional wire bond equipment and processes with advanced thinning technologies, STATS ChipPAC is able to offer a leading edge solution that still satisfies the cost sensitive demands of consumer applications: **Extremely Thin Profile Array Packaging** solutions. STATS ChipPAC's extremely thin packages offer maximum profile heights less than 0.50mm.

While bare die solutions have typically been utilized for extremely thin profile requirements, STATS ChipPAC now offers the option of using a substrate based molded package for the same applications. These extra thin packages are able to accommodate die shrinks without changing the package footprint as well as integrate more than one device within the package.

In order to achieve a maximum profile height less than 0.50 mm, STATS ChipPAC utilizes a 0.13 mm two metal layer laminate substrate, wafer thinning down to 75 microns, advanced molding technology, and an optimized bill of materials to minimize warpage of the assembled package.

STATS ChipPAC's extra thin design allows a full array of solder balls or lands on the substrate to deliver greater flexibility in input/output (I/O), layout and density in a given package size. STATS ChipPAC's Extremely Thin Fine Ball Grid Array (XFBGA) package features a maximum height of 0.50 mm while the Extremely Fine Land Grid Array (X1FLGA) package achieves a maximum height of 0.45 mm

Extremely Thin Profile Array Packages

XFBGA, XFLGA, X1FLGA

SPECIFICATIONS

Die Thickness	75-100µm (3-4 mils)
Mold Cap Thickness	0.25-0.30mm
Marking	Laser
Packing Options	Tape & Reel; JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (-65°C to 150°C), 1000 cycles
High Temp Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C/100% RH/2atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

THERMAL PERFORMANCE, θ_{ja} (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance θ_{ja} (°C/W)
XFBGA	11 x 11 (2L)	144	4.5 x 4.5	46.48

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

ELECTRICAL PERFORMANCE

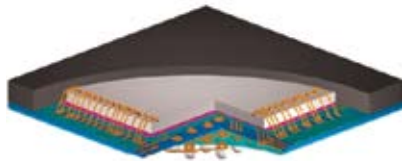
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	25 - 110	1.10 - 4.35	0.25 - 2.27	0.20 - 0.90	0.05 - 0.41
Total (2L)	4 - 0	145 - 230	2.75 - 6.00	0.70 - 3.12	0.30 - 1.00	0.06 - 0.43

Note: Net = Total Trace Length + Via

CROSS-SECTION

XFBGA



XFLGA



PACKAGE CONFIGURATIONS

Package Size (mm)	Ball Count
Body Sizes (mm)	4 x 4 to 15 x 15
Terminal Count	8 to 200+
Terminal Pitch (mm)	0.50 to 0.80
Typ. Pkg. Thickness	XFBGA: 0.50mm max. XFLGA: 0.50mm max. X1FLGA: 0.45mm max.

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