STATSChipPAC®

SPM-T

Simplified Package Modeling - Thermal

Simplified Package Modeling

Demand continues to grow and time-to-market pressures have intensified for complex package designs that grow larger and more complex with each generation of devices. Also increasing is the demand for non-symmetrical, stacked die and other multi-chip packages. To meet these needs, STATS ChipPAC has developed a leading-edge approach to thermal modeling called Simplified Package Modeling (SPM) that provides customers with unmatched design flexibility, early confirmation of thermal performance and a significant potential reduction of design cycle time.

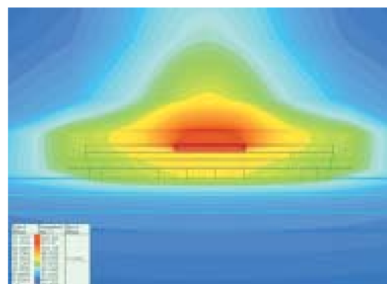
Rather than waiting until the end of a design cycle to perform thermal analysis, STATS ChipPAC recognizes the benefit of having early and flexible thermal models that provide customers with thermal information at multiple points in the design cycle. STATS ChipPAC's technique allows an initial SPM to be performed as soon as a customer identifies the basic package design requirements: package type, die size, number of solder balls, copper layers, etc. No need to complete the final design of the substrate or lead frame.

The SPM technique relies on creating a simplified model that matches an experimentally tested design, and is similar to but not identical to the customer design. The simplifications involve combining discrete elements within the package, such are traces, bond wires or lead frame fingers, into larger blocks of material. These cuboids are each then assigned an "effective" thermal conductivity that produces the correct thermal behavior during the simulation process. Other materials within the package that are thin, such as the die attach adhesive layer, are collapsed into a zero thickness layer that produces an appropriate resistance to the passage of heat. The models utilize a simulation domain that matches JEDEC standards for thermal testing.

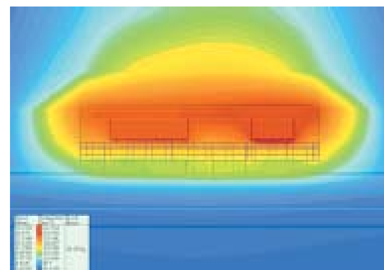
In addition, the underlying PCB test board is also simulated, allowing STATS ChipPAC to simulate the effect of modifications to the design. If applicable, STATS ChipPAC can also include any type of heat sink that might be required by the customer.

These initial models are then correlated with the corresponding experimental results from the STATS ChipPAC thermal database. This correlation involves making educated adjustments based on experience and heat transfer expertise to the properties and geometry of the simplified cuboids until the results are within 2% of the experimental data. The design details (die size, ambient temperature, power dissipation, etc.) are then modified to match the preliminary details of the customer design. Using this process, STATS ChipPAC has consistently obtained results that are accurate to within 5% of the actual thermal resistance determined by subsequent testing of the final devices.

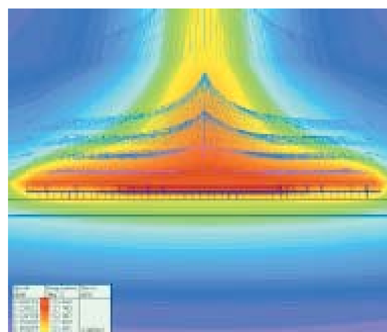
Initial simulation results, generally available within 1 or 2 days of receiving the initial design information, are used



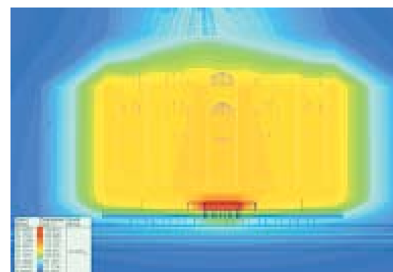
Stacked die thermal behavior



Thermal behavior of two flip chip die with spreader across top



Large EBGA package thermal behavior



Thermal behavior of LFBGA package with heat sink

STATSChipPAC®

SPM-T

Simplified Package Modeling - Thermal

to verify that the proposed package type meets the needs of this project. If a thermal problem exists, it will be identified very early in the design process so that appropriate changes can be made. In the absence of any thermal problems, the final package design process continues without delay. As the final design is completed, the initial model can be modified for any changes of thermal consequence, and a final prediction of thermal behavior is provided to the customer.

Package Size and Complexity

Another advantage of SPM occurs when simulation is required for very large and/or complex package designs. The internal design simplifications result in a dramatic decrease in computing resources. When conventional simulation techniques are used, the detailed internal design information of relatively simple semiconductor packages can overwhelm the capabilities of even the best software. To overcome this, it is common practice to section designs along planes of symmetry and perform simulation on a small section of the actual package. It is typical to simulate only a 1/4 or 1/8 section of the full design.

However, as package size and complexity continues to increase, these symmetric simplifications can prove insufficient. In particular, there are many new designs that with limited symmetry: multiple die packages, stacked die packages, on-package passives, etc. These situations create difficulty for detailed package modeling techniques.

Using STATS ChipPAC's SPM technique, the package is modeled in its entirety. The internal simplifications allow even the most complex packages to be fully modeled within a domain that simulates that of an experimental test chamber.

In addition, STATS ChipPAC's SPM technique allows simulation of the underlying PCB, and can accommodate for design modifications such as thermal vias.

Experimental Capabilities

STATS ChipPAC's experimental test capabilities include:

- **Natural convection testing to JEDEC JC51-2**
- **Forced convection testing to JEDEC JC51-6**
- **Testing with thermal die or active devices**

STATS ChipPAC has thermal test labs at its Singapore and Korea factories

Resistor Network Compact Models

Once the detailed package model is completed, it can be converted into a Resistor Network Compact Model that follows the Delphi 6 node format. The result is a boundary condition independent model that can be used for system level modeling in any software tool that is capable of using resistor network models. Accuracy is very good, typically less than 2% error when compared to the detailed package model.

Thermal Test Database

A key element to the successful implementation of SPM is the availability of experimental test results for a large variety of package designs and configurations. STATS ChipPAC has an extensive database of package tests performed under JEDEC standard conditions for natural and forced convection.

Summary

Since implementing the SPM approach, STATS ChipPAC has been able to provide unique benefits to our customers including:

- Accurate thermal resistance data to customers on average 1-2 days from receipt of general package information without the need to wait for final design drawings.
- Simulations correlated to experimental data generated under JEDEC testing standards.
- Full package simulation regardless of size, complexity or lack of symmetry and including underlying PCB and heat sink if applicable.
- Design cycle time has, in some cases, been dramatically reduced because thermal analysis was completed in parallel with the final package layout and design.
- Resistor Network Compact Models provided to customers upon request.

Corporate Office 10 Ang Mo Kio St. 65, #05-17/20 Techpoint, Singapore 569059 Tel: 65-6824-7777 Fax: 65-6720-7823
Global Offices USA 510-979-8000 JAPAN 81-3-5789-5850 CHINA 86-21-5976-5858 MALAYSIA 603-4257-6222
KOREA 82-31-639-8911 TAIWAN 886-3-601-5858 UK 44-1483-413-700 NETHERLANDS 31-38-333-2023

The STATS ChipPAC logo is a registered trademark of STATS ChipPAC Ltd. Trademark registered in the United States. Singapore company registration number 199407932D. All other product names and other company names herein are for identification purposes only and may be the trademarks or registered trademarks of their respective owners. STATS ChipPAC disclaims any and all rights to those marks. STATS ChipPAC makes no guarantee or warranty of its accuracy in the information given, or that the use of such information will not infringe on the intellectual rights of third parties. Under no circumstances shall STATS ChipPAC be liable for any damages whatsoever arising out of the use of, or inability to use the materials in this document. STATS ChipPAC reserves the right to change the information at any time and without notice. ©Copyright 2007. STATS ChipPAC Ltd. All rights reserved.
November 2007