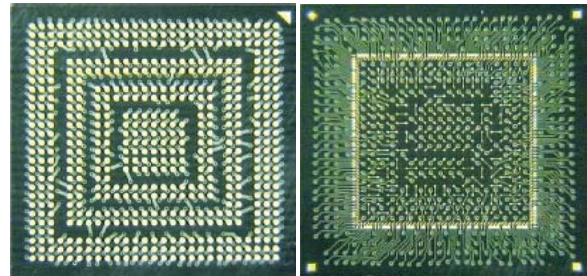
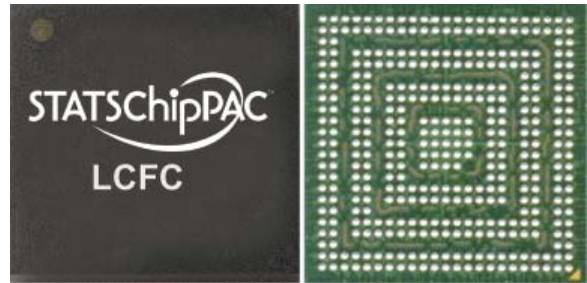


# Low Cost Flip Chip (LCFC)

fcBGA, fcFBGA, fcLGA, fcFBGA-SD

## HIGHLIGHTS

- Routing-efficient interconnection structure & optimized bump layout help "fit" flip chip designs into low cost laminate substrates
- Mold underfill (MUF) process technology
- Elimination of Solder-on-Pad (SOP) process on substrates
- High throughput processing through combination of high UPH unit processes, optimization of material flow & equipment selection
- High density matrix strip for fcFBGA & wide boat format for singulated substrate handling for fcBGA
- Smaller package size & lower electrical parasitics achievable compared with corresponding wire bond package options
- LCFC package cost below wire bond package cost
- Applicable across full range of fcBGA & fcFBGA package families



## FEATURES

- Sn-Pb, Sn-Ag (Pb-free) and Cu column bumps
- Bumped wafer thinning: 100µm Si thickness in production, 75µm qualified
- Conventional 2/4 layer laminate, laminate Build-up (BU) & ABF BU substrates
- 150µm bump pitch in production, 80µm in development with Cu column bump
- 0.40mm minimum package ball (BGA) pitch in production
- Package body sizes ranging from 4 x 4mm through 45 x 45mm
- In-house wafer bumping with plated & printed bumps for 200 & 300mm wafers
- Mold underfill (MUF) with solder bump in production, with Cu column bump in qualification

## APPLICATIONS

Devices primarily for wireless and portable products such as RFICs and power/analog ICs driven by miniaturization and low package parasitics, and for ASIC, graphics and computing products driven by superior electrical and thermal performance.

## DESCRIPTION

STATS ChipPAC's Low Cost Flip Chip (LCFC) packages form a subgroup in the Flip Chip package family which represents any flip chip platforms that leverage cost saving features such as nSOP (no Solder on Pad), MUF (mold underfill) and BOL (bond on lead) interconnection to name a few.

LCFC packages are produced on substrates with matrix strip or singulated format, and use overmolding and saw singulation processes for strip base substrate similar to wire bond packages of the same form factor. The fcBGA is typically an exposed die package with CUF (capillary underfill); fcFBGA is typically an overmolded package; both fcBGA and fcFBGA use solder balls for second level (BGA) interconnection; fcFBGA-SDx represents a variation of fcFBGA comprising a "hybrid" stacked construction, i.e., flip chip die on the bottom and wire bond die on the top; while the fcLGA is an exposed die product that does not have solder balls.

STATS ChipPAC's LCFC packages are available in ball counts ranging from 32 to > 1000 depending on body size and external terminal (BGA) pitch. Other features such as heat spreaders for thermal enhancement, surface mounted passive components, etc. that are offered with traditional fcFBGA and fcBGA packages are also available for LCFC packages.

Flip Chip interconnection provides the ultimate in miniaturization and reduced package parasitics and enables new paradigms in the area of power and ground distribution to the chip which are not feasible with traditional wire bond packaging. STATS ChipPAC offers full turnkey services ranging from design through production, including high speed, high pin count digital and RF testing.

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## SPECIFICATIONS

Package Thickness	0.65-2.9mm
Die Thickness	200mm wafers: 100-710µm (4-28mils) 300mm wafers: 100-810µm (4-32mils)
Bump Pitch	150µm (production) 80µm (development)
Marking	Ink or laser

## RELIABILITY

Moisture Sensitivity Level	JEDEC Level 3 @ 260°C
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiased HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

## THERMAL PERFORMANCE

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation and/or measurement for specific cases should be performed for maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Perf. ja θ°C/W
fcLFBGA	7 x 7	49	4.6 x 5.0	46.0
fcLGA	13 x 13	144	5.5 x 5.5	27.7
fcBGA-H	40 x 40	1161	12.8 x 12.8	11.2/8.0* (8.4 / 4.4*)

Note: Simulation data based on package mounted to 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2; \* represents cases with extruded Aluminium heat sink; numbers in parentheses are for 2 m/sec air flow and provided for reference for applications that provide fans or other forms of air flow in the system.

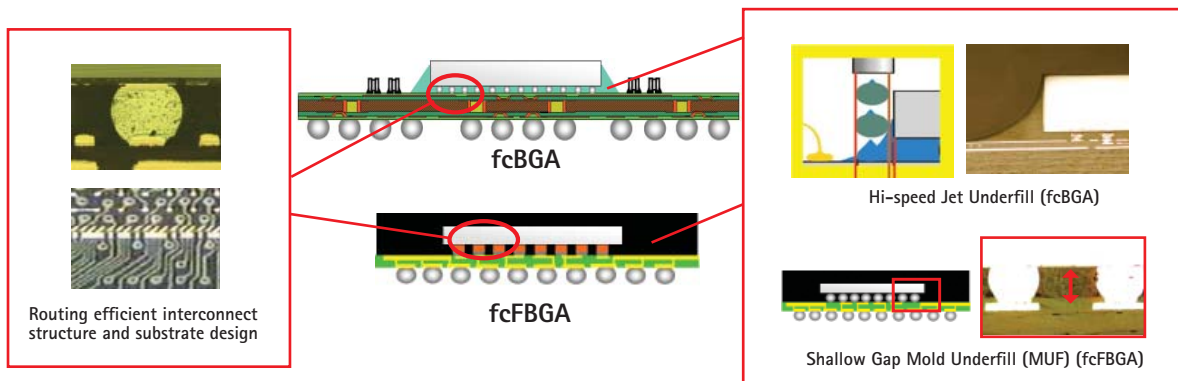
## ELECTRICAL PERFORMANCE

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz.

Package	Body Size (mm)	Die Size (mm)	Length	Inductance (nH)	Capacitance (pF)	Resistance (mΩ)
fcLFBGA	13 x 13	6.0 x 8.0	Self (short)	0.89	0.65	18.3
			Mutual	0.24	0.11	
			Self (long)	1.78	0.73	32.5
			Mutual	0.51	0.12	

Note: Net = Total Trace Length + Via + Solder Ball.

## CROSS-SECTION



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