



台灣星科金朋半導體股份有限公司

STATS ChipPAC Taiwan Semiconductor Corporation

Your Wafer and IC Testing Partner in Taiwan

Finding the right test solution to meet your needs is essential in today's competitive market. As one of the leading test houses in Taiwan, STATS ChipPAC Taiwan Semiconductor Corporation offers proven expertise in mixed-signal, digital, embedded memory, consumer optics and wireless applications. With a strategic and long standing relationship to TSMC, STATS ChipPAC Taiwan Semiconductor Corporation is well prepared to serve as a part of your global supply chain. Our portfolio of advanced test platforms and experienced R&D and engineering teams can reduce your engineering burden and ready your product for commercial success in the shortest time possible.

Quality and time-to-market are two of the critical factors in the success of your product. To ensure you receive the highest level of quality, STATS ChipPAC Taiwan has achieved top industry certifications including ISO9001, ISO14001 and OHSAS18001.

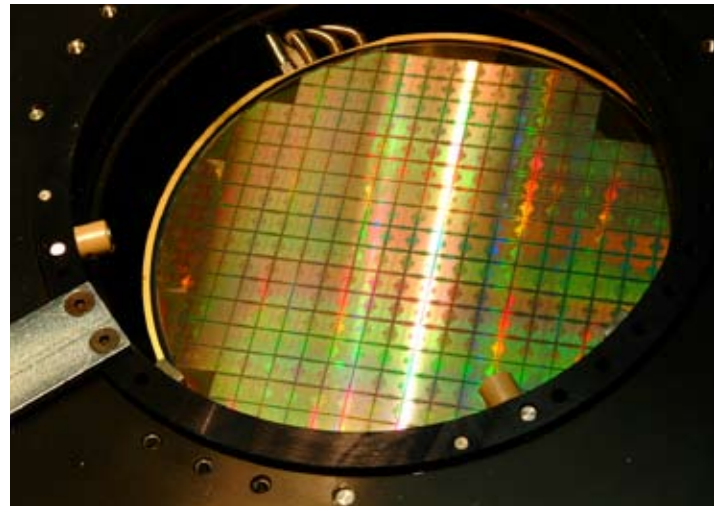
Turnkey Test Services

STATS ChipPAC Taiwan Semiconductor Corporation offers a full spectrum of turnkey services including:

- Incoming inspection
- Wafer probe / bumped wafer probe
 - 200mm - 300mm wafer probe / bumped wafer probe
 - Vertical wafer / bumped wafer probe
 - Laser trim
- Final test
- Dry-bake, packing, tape and reel
- Drop shipment to your end customer

Bump Services

Offering state-of-art-technology, STATS ChipPAC's Taiwan bumping facility provides eutectic and solder alloy (low alpha) and leadfree soldering bumping.



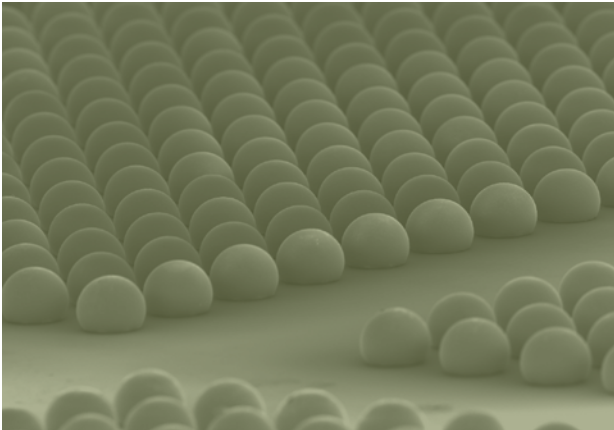
CMOS Image Sensors

In 2004, we unveiled our testing service for CMOS Image Sensor (CIS) devices. STATS ChipPAC Taiwan is the clear market leader in Taiwan.

We offer the right combination of experience, services and quality to help your company and your product succeed in the global economy.

Test Platforms

Manufacturer	Model	System Capability
Advantest	T2000	Mixed-Signal
Credence	SC312	50 MHz Logic
Teradyne	I-Flex	Mixed-Signal
Teradyne	I-Flex RF	RF & Mixed-Signal
Teradyne	UltraFlex	Mixed-Signal
Teradyne	Catalyst	Mixed-Signal
Teradyne	J750	100 MHz Logic
Verigy	93000	Mixed-Signal
Verigy	94000	Mixed-Signal
Verigy	PS800	Mixed-Signal
Verigy	PS400	Mixed-Signal
Verigy	PS400 (Portscale)	RF & Mixed-Signal



Wafer Bumping

Wafer bumping is a process in which interconnections (solder “bumps” or “balls”) are formed on an entire wafer prior to dicing. The use of wafer bumping is driven either by performance, form factor or array interconnect requirements and can offer significant technical and cost advantages over traditional single-die packaging. The need for high performance, high I/O densities and efficient on-chip power distribution schemes that are unattainable by conventional wire bonding interconnection, has led wafer bumping to replace wire bonding as the interconnection of choice for a growing number of components.



12” Solder Bump Services at STATS ChipPAC Taiwan

STATS ChipPAC’s Taiwan world-class solder bumping line offers HVM production capability for 300mm wafers. This state-of-the-art facility provides eutectic and solder alloy (low alpha) and leadfree soldering bumping.

Process Capability

Technology	Plating bump (300mm)
Bump material	Eutectic & Pb Free (Ultra Low Alpha)
Solder material	Sn63/Pb37 (Eutectic)
	Sn98.2/Ag1.8 (Pb Free)
UBM Structure	Sputter Ti/Cu and Plating Cu/Ni
Minimum bump pitch	150 μ m
Bump height & size	80 μ m / 100 μ m
Wafer Probe Test	Available

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STATS ChipPAC Taiwan Semiconductor Corporation

No. 176-5, Lu Liao Ken, 6 Ling, Hua Lung Chun, Chiung Lin

Hsin-Chiu Hsien, Taiwan, R.O.C. 307

Tel: 886-3-593-6565 / Fax: 886-3-593-6363

www.statschippac.com.tw