

fcPiP

Flip Chip Package-in-Package: LFBGA-PiPs-SDx + y

HIGHLIGHTS

- Combines flip chip and wirebond interconnection for ultimate in performance and functional integration
- Package-in-Package configuration facilitates use of pre-tested memory and high module yields
- Mechanical form, fit and function identical to JEDEC standard FBGA packages

FEATURES

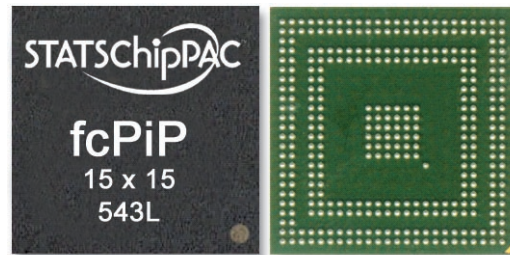
- Package/die stack: 1 flip chip die + 1 ISM + 1 or more bare wirebondable die
- Package/die and passive component integration: 2 flip chip die side by side + ISM + passive component
- 10 x 10mm to 23 x 23mm body sizes
- Package body size can equal ISM LGA size + 2mm
- Overall package height including solder balls at 1.2mm and 1.4mm max
- 0.4mm to 0.8mm ball pitch
- Flip chip with 28/45nm Si node ELK and lead-free bump
- Logic, Memory and Analog functions can be combined
- JEDEC standard package outlines available for ISM & FBGA
- Thin die capability down to 100µm Si thickness
- Thin mold cap down to 200µm for ISM LGA
- Higher memory capacity ISM from 256MB to 512MB/1GB
- Low loop wirebonding, <50µm
- BOL, nSOP, MUF for lower package cost structure

APPLICATIONS

- Portable electronics (Cellular phones, Gaming, PDAs, Digital Cameras, Camcorders, Wireless products)
- Integration of digital base band, memory and analog functions in a high end cellular handset architecture
- Mixed technology integration at package level (SIP) as a trade off for SOC designs where die yields are compromised by Si-level integration of disparate functional blocks
- Any 3D application requiring the use of flip chip interconnection for performance reasons

TEST SERVICES

- Product Engineering support
- Probe capability
- Program generation/conversion
- Drop Ship available



DESCRIPTION

fcPiP is an innovative family of 3D packages that stack minimally packaged die and bare die into a single molded package. A pre-tested Internal Stacking Module (ISM) Land Grid Array (LGA) and one or more bare die are stacked with at least one bare die connected to the substrate using flip chip interconnection. The flip chip die is underfilled using a special fine fillet underfilling process. The ISM is inverted and attached to the top surface of the Flip Chip device leaving exposed bond fingers for subsequent wirebond interconnection to the base substrate. The wirebondable bare die is attached onto the top surface of the ISM-LGA. Finally both the ISM-LGA and bare die are wirebonded to a common base substrate. This is followed by a single step overmolding process.

A typical fcPiP integrates an ASIC or DSP logic device (generally with flip chip interconnection) with memory die(s) (in the ISM configuration) and analog die(s) (in bare die configuration), the latter two interconnected to the common substrate using wire bond interconnection. A typical package could have a footprint of 15x15 mm, 1.4mm maximum thickness and incorporate a 0.5 or 0.4mm ball pitch.

ADVANTAGES

3D packaging is driven by wireless and consumer products that require package level functional integration in the smallest footprint, lowest profile and lowest cost. Stacked die packages for Flash, SRAM and DRAM memories in an FBGA package footprint using wirebond interconnection are widely available today. However, with the onset of more complex device designs, two new challenges have arisen: (a) higher I/O density and performance requirements on logic chips dictate the use of flip chip interconnection, and (b) the complexity of memory chips makes it difficult to obtain them in "known good die (KGD)" form.

fcPiP addresses these concerns: the use of flip chip interconnection for the logic die addresses the need for high I/O density and low parasitics, while the procurement of memory in the form of pre-tested ISM packages ensures that the memory devices are "known good."

An additional benefit is the high level of reliability made possible by the overmolded structure which is typically superior to flip chip-only packages. In addition, the fcPiP configuration obviates certain problems associated with the competing configuration known as fcPoP, such as warpage management and SMT process difficulties associated with mounting the PoP top and bottom packages.

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STANDARD MATERIALS

Flip Chip	Eutectic Hi Pb or Pb-free bump; 160µm Et 180µm min pitch
Substrate	Through-hole laminate (e.g., BT-832HS) or laminate build-up (BU)
Wire	20-25µm (0.8 - 1.0mil) diameter Au wire
Mold Compound	Epoxy Resin
Solder Ball	SnPb or SAC (Pb-free)
Package Options	JEDEC tray or tape Et reel

RELIABILITY (Preconditioning Level @ 260°C 3xIR reflow)

Moisture Sensitivity Level	JEDEC Level 2aa (60°C/60%, 120 hrs)
Temperature Cycling	Condition B (-55 to 125°C) w/Precon, 1000 cycles
Temp/Humidity Test	85°C/85% RH, 1000 hrs
Highly Accelerated Stress Test	135°C/85% RH, 96 hrs
High Temp Storage	150°C, 1000 hrs

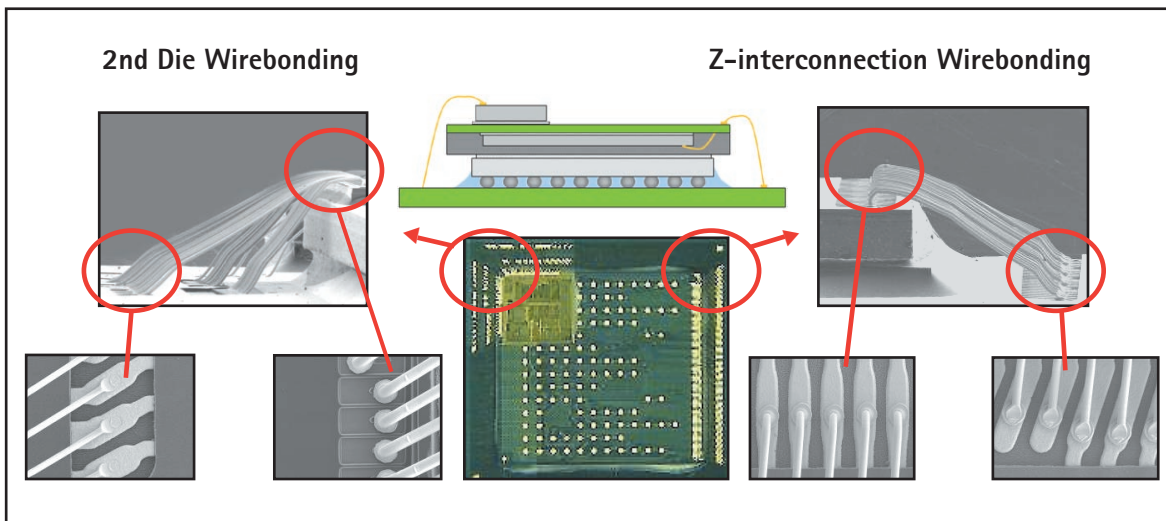
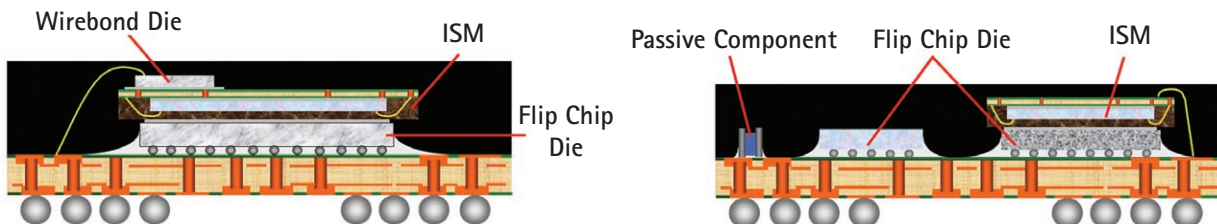
PROCESS HIGHLIGHTS

Stacking	Typical stack: 1 flip chip die+1 ISM+1-3 bare die (wirebondable); ISM can have 1-4 die stack internal to the ISM
Wafer Thinning	100µm Si thickness (75µm in development) for flip chip die, 60µm for wirebond die
Die Overhang	ISM LGA can have up to 2mm overhang
Molding	Down to 0.20mm mold cap for ISM LGA
Marking	Laser

PACKAGE CONFIGURATIONS

Typical Body Sizes	13x13, 14x14, 15x15, 16x16mm
Available Body Sizes	Up to 23x23mm
Ball Count	543, 603 (tooled); higher ball count available
Ball Pitch	0.4 to 0.8mm
Pkg Thickness	1.4mm based on 1 flip chip+1 ISM+1 bare die (wirebonded) 1.2mm based on 2 flip chip + 1 ISM + passive component

CROSS-SECTIONS



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