

TSOP

Thin Small Outline Package

- **Body Sizes:** 12 x 20mm (48 lead);
14 x 20mm (56 lead)
- **Lead Pitch:** 0.50mm
- **Stacked Die:** available between 2 to 4 die
- **Stacking Options:** same size die, staggered, staircase, pyramid



FEATURES

- Two body sizes available in TSOP type 1 version
- Lead counts: 48 and 56
- Lead pitch: 0.50mm
- Wide range of open tool die pad sizes available; custom size available
- Moisture sensitivity: JEDEC Level 3
- JEDEC standard compliant
- Lead-free (Pb free) and green material sets available
- Copper and alloy 42 leadframes available
- Die stacking available up to 4 die

APPLICATIONS

- Memory
- RF / Wireless
- Logic and Linear
- End applications including portable electronics, memory modules and networking equipment

DESCRIPTION

STATS ChipPAC offers the Thin Small Outline Package (TSOP). Reliability and thin profile are key TSOP attributes using surface mount technology (SMT). TSOP is available in a thermally enhanced version (TSOP-ep), as well as a stacked die version (TSOP-SD). Die stacking is available from 2 to 4 die, with bonding pads on two sides of the die or single-sided bonding pads.

STATS ChipPAC uses the latest leadframe technology and state of the art design and simulation tools to achieve optimum electrical and thermal performance. STATS ChipPAC's state of the art assembly facility and proven materials assure high yield manufacturing and long term reliability.

Thin Small Outline Package

SPECIFICATIONS

Single Die Thickness	10-12mils
Stacking Die Thickness	75µm (3mils) minimum
Gold Wire	0.8mils diameter, 99.99% Au
Lead Finish	Matte Tin
Marking	Laser
Packing Options	JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	-65°C/150°C, 1000 cycles
Temp/Humidity Test	85°C/85% RH, 1000 hrs
Pressure Cooker Test	121°C 100% RH, 2 atm, 250 hrs

THERMAL PERFORMANCE, θ_{ja} (°C/W)

Package	Body Size (mm)	Die Size (mils)	Thermal Resistance θ_{ja} (1.0W, natural convection)
48L TSOP	12 x 20	150 x 150	60°C/W
48L TSOP	12 x 20	100 x 100	75°C/W

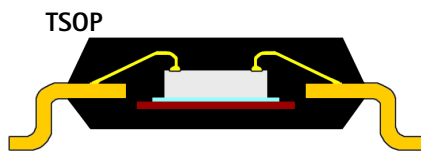
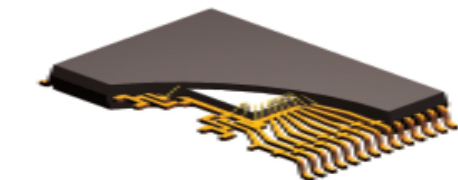
Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-5) under natural convection as defined in JESD51.2.

ELECTRICAL PERFORMANCE: TSOP 48L

Conductor Component	Body Size (mm)	Lead/Wire (mm)	Resistance (mOhm)	Inductance		Capacitance	
				Self (nH)	Mutual (nH)	Self (pF)	Mutual (pF)
Lead	12 x 20	6.56-7.60	38.0-44.0	3.49-4.17		0.69-0.87	
Wire		1.90	114	1.58		0.08	
TOTALS			152-158	5.07-5.75	2.32-2.63	0.77-0.95	0.36-0.39

Note: Results are simulated values at 100MHz.

CROSS-SECTIONS

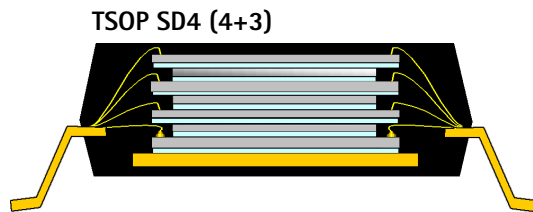


TSOP-SD2 (2+0) staircase



PACKAGE CONFIGURATIONS

Package	Body Size	Lead Count
TSOP	12 x 20mm	48
	14 x 20mm	56



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