

SiP

System-in-Package

HIGHLIGHTS

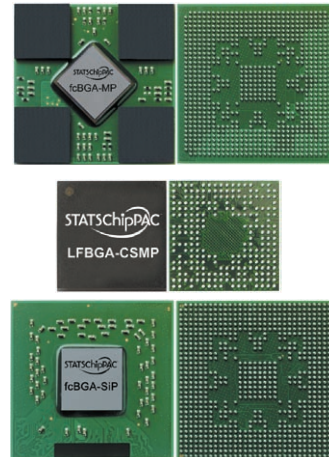
- Reduced Development Time & Cost
- Mixed IC Technology and SMT Components
- Standard and Green Materials Set
- Multi-die, Side-by-Side & Stacked
- Flip Chip and Wirebond

FEATURES

- Body sizes up to 50 x 50mm
- Flexible ball and land grid arrays
- Lead-free and green materials set
- Multiple routing layers and dedicated ground/power planes available for improved electrical performance
- BT laminate materials, Si backplane
- JEDEC standard compliant

APPLICATIONS

- RF/Wireless: Power amplifiers, baseband, transceiver modules, Bluetooth™, GPS, UWB, etc.
- Consumer: Digital cameras, handheld devices, memory cards, etc.
- Networking/Broadband: PHY devices, line drivers, etc.
- Graphics processors



DESCRIPTION

STATS ChipPAC's System in Package (SiP) is a substrate based package with one or more IC's, multiple passives and other surface mount components with plastic overmolded encapsulation. The use of advanced assembly techniques, such as flip chip, die stacking or a combination of both, allows mixed technology IC's and other components to be combined in a cost effective and reliable package with minimal footprint and maximum functionality. In addition, this package can be built either as a Land Grid Array or Ball Grid Array to match the application or thermal/electrical design requirements.

ADVANTAGES

SiP is an excellent alternative to SoC (System-on-Chip). SoC can be difficult to design and build as different functions are combined on one fab technology. SiP can combine multiple die (manufactured using different wafer fabrication processes) without performance tradeoffs, reducing time to market, development costs and expanding the supply chain.

SiP also provides an excellent solution for ease of system level manufacturability and design. By including critical components into the SiP package and moving routing to the SiP, the system complexity, size and component placements can be reduced.

System-in-Package

SPECIFICATIONS

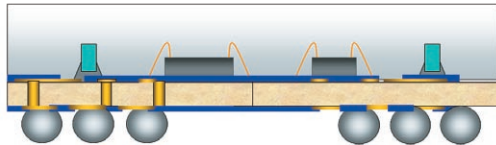
| | |
|-----------------|---|
| Die Thickness | 60 - 355µm (2.4 - 14mils) |
| Gold Wire | 0.6 - 1.3mil diameter, 99.99% Au |
| SMT Components | 0603, 0402, 0201, 01005, odd parts, x-tals, filters, etc. |
| BOM | Standard and lead-free |
| Marking | Ink/laser |
| Packing Options | JEDEC tray/tape and reel |

RELIABILITY

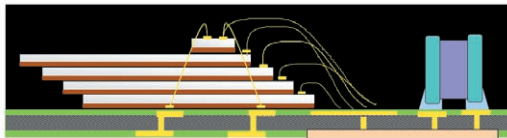
| | |
|----------------------------|--------------------------------|
| Package Level | |
| Moisture Sensitivity Level | JEDEC Level 3 |
| Temperature Cycling | -65°C ~ 150°C, 500/1000 cycles |
| High Temperature Storage | 150°C, 1000 hrs |
| Pressure Cooker Test | 121°C/100%RH/2atm, 168 hrs |
| Temperature/Humidity Test | 85°C/85% RH, 1000 hrs |
| Unbiased HAST | 130°C/85% RH/33.3psia |
| Board Level | |
| Test Vehicle | 10x10, 72 LGA-SiP |
| Model | MO-208 |
| Design | Daisy Chain by Wirebond |

CROSS-SECTIONS

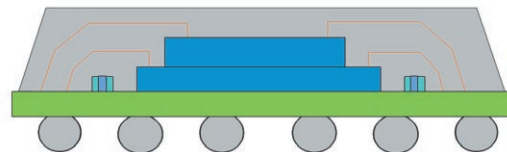
PBGA-SiP



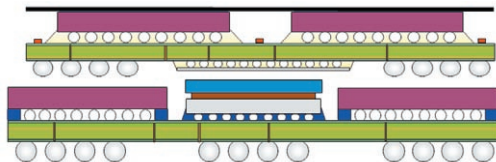
LFBGA-SiP-SD



PBGA-SiP-SD



fcBGA-MP-SiP

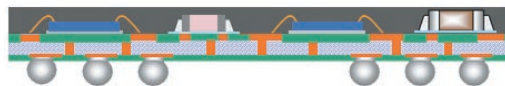


PACKAGE CONFIGURATIONS

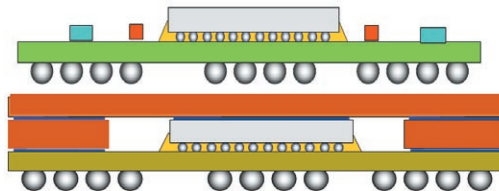
A variety of Wirebond, Flip Chip and Stacked Die configurations are in production and under development. In addition, many standard package configurations can be integrated to address customer specific solutions.

Contact your local STATS ChipPAC sales representative for additional information.

LFBGA-SiP



fcBGA-H-SiP



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