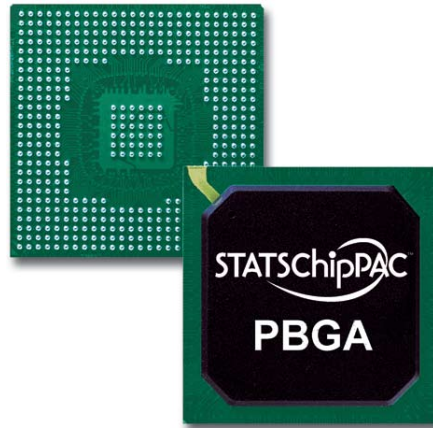


PBGA

Plastic Ball Grid Array

- Strip molded, cost effective, high I/O package solution
- Wide range of tooled up body sizes for minimum cost of entry
- Available in Pb-free and eutectic versions



FEATURES

- Full in-house package and substrate design capability
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Multiple metal layer options for signal, power and ground planes for improved electrical performance
- Wide range of custom and open tool designs available
- Flexible body sizes ranging from 15 x 15mm to 40 x 40mm
- 0.80, 1.00, 1.27 and 1.50mm ball pitch with greater than 1000 I/O available
- Perimeter or full ball array
- Pb-free and green material set options
- Multiple chip design and optional passive/discrete components available (SiP)
- JEDEC standard compliant

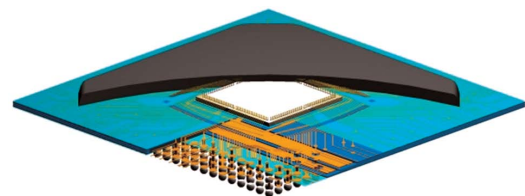
APPLICATIONS

- ASIC
- DSPs and Memory
- Gate Array
- Microprocessors/Controllers/Graphics
- PC Chipsets
- Other advanced applications requiring enhanced thermal and electrical performance

DESCRIPTION

STATS ChipPAC's Plastic Ball Grid Array (PBGA) packages utilize laminate substrates and are available over a variety of standard JEDEC body sizes and ball counts to meet a wide range of customer requirements. This package provides a cost-effective advanced packaging solution, offering higher density over traditional leadframe packages. STATS ChipPAC's advanced design and simulation capabilities enable package optimizations needed for maximum electrical and thermal performance. STATS ChipPAC combines state of the art processing and equipment with proven material sets to achieve enhanced yield, reliability, and performance. Green and lead-free material sets are available for all PBGA package types.

CROSS-SECTION



PBGA

Plastic Ball Grid Array

SPECIFICATIONS

Die Thickness	150-381µm (6-15mils)
Gold Wire	18-30µm (0.7/0.8/0.9/1.0/1.2mils) diameter
Bond Pad Pitch	45µm inline or 25/50µm staggered capable
Marking	Laser
Packing Options	JEDEC tray/tape and reel

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	-65°C/150°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Pressure Cooker Test	121°C, 100%RH, 2 atm, 168 hrs
Liquid Thermal Shock	(Condition B) -55°C/125°C, 1000 cycles

THERMAL PERFORMANCE, θ_{ja} (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Ball Count	Die Size (mm)	Thermal Performance θ_{ja} (°C/W)
27 x 27	2L	256	7.8 x 7.8	29.8
27 x 27	4L	256	7.8 x 7.8	22.4
27 x 27	4L	272	7.8 x 7.8	20.2
35 x 35	4L	388	10.2 x 10.2	15.9

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

ELECTRICAL PERFORMANCE

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.1	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.3 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)		154 - 239	2.95 - 6.2	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Wire	2	120	1.65	0.45 - 0.85	0.1	0.01 - 0.02
Net (4L)	2 - 7	34 - 119	0.9 - 3.15	0.18 - 1.58	0.35 - 1.1	0.06 - 0.42
Total (4L)		154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.2	0.07 - 0.44

Note: Net = Total Trace Length + Via + Solder Ball.

PACKAGE CONFIGURATIONS

Body Size (mm) Ball Count

15 x 15	160, 176, 196
17 x 17	192, 196, 208, 217, 252, 256
19 x 19	272, 289, 292, 296, 297, 300, 301, 305, 324, 376
21 x 21	400, 456, 484
23 x 23	169, 192, 208, 217, 233, 241, 288, 301, 304, 305, 318, 320, 324, 338, 340, 348, 352, 360, 376, 385, 388, 420, 456, 480, 484, 492
27 x 27	225, 256, 272, 277, 292, 300, 312, 316, 320, 324, 336, 352, 384, 388, 400, 416, 456, 472, 480, 484, 496, 508, 512, 544, 580, 585, 636, 650, 676
31 x 31	304, 320, 353, 385, 421, 433, 434, 448, 458, 460, 480, 540, 556, 560, 564, 604, 608, 609, 640, 644, 652, 676, 688, 692, 701, 721, 772, 896
35 x 35	304, 312, 313, 340, 352, 385, 388, 400, 420, 426, 432, 448, 452, 454, 456, 458, 474, 480, 484, 492, 496, 512, 516, 532, 542, 544, 548, 556, 564, 573, 580, 611, 624, 640, 648, 661, 665, 676, 680, 688, 700, 716, 729, 736, 740, 748, 756, 792, 816, 824, 840, 867, 868, 1012, 1156
37.5 x 37.5	435, 480, 552, 600, 601, 625, 627, 685, 701, 785, 788, 804, 840, 841
40 x 40	503, 557, 569, 596, 600, 745, 776, 928, 961, 1253

Corporate Office 10 Ang Mo Kio St. 65, #05-17/20 Techpoint, Singapore 569059 Tel: 65-6824-7777 Fax: 65-6720-7823

Global Offices USA 510-979-8000 JAPAN 81-03-3507-5676 CHINA 86-21-5976-5858 MALAYSIA 603-4257-6222
KOREA 82-31-639-8911 TAIWAN 886-3-593-6565 UK 44-1483-413-700 NETHERLANDS 31-38-333-2023

The STATS ChipPAC logo is a registered trademark of STATS ChipPAC Ltd. Trademark registered in United States. Singapore company registration number 199407932D. All other product names and other company names herein are for identification purposes only and may be the trademarks or registered trademarks of their respective owners. STATS ChipPAC disclaims any and all rights in those marks. STATS ChipPAC makes no guarantee or warranty of its accuracy in the information given, or that the use of such information will not infringe on intellectual rights of third parties. Under no circumstances shall STATS ChipPAC be liable for any damages whatsoever arising out of the use of, or inability to use the materials in this document. STATS ChipPAC reserves the right to change the information at any time and without notice. ©Copyright 2010. STATS ChipPAC Ltd. All rights reserved. March 2010