

# **“Comparison of Advanced PoP Package Configurations”**

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## Comparison of Advanced PoP Package Configurations

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### Abstract

The continued demand for higher level of integration has led to the industry's adoption of 3D packaging technologies and, in particular, the Package-On-Package (PoP) configurations. This technology allows for vertical integration of the memory package and the logic package into one stacked package. The top package is primarily a memory module including some combination of Flash and SDRAM, while the bottom package typically contains the logic die, which is a baseband or an application processor of some kind. Top and bottom package are connected via the pads that are located on the top side of the bottom PoP package, and these pads are used to connect the top PoP (memory module) Ball Grid Array (BGA) solder balls to the bottom PoP package. This paper details the various PoP package types including bare-die PoP, Embedded Solder On Pad (eSOP) PoP, and Laser-Via PoP that have proliferated to meet the increasing market demand. Also, the various package types are compared to each other in terms of their feasibility for adoption in the next generation PoP with tighter pitch and lower package profile.

### PoP Package Types

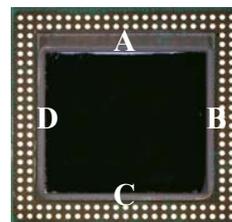
Original PoP packages were designed in wire-bonded configuration and hence the die in bottom package was encapsulated in mold compound to protect the wires. This molding would cover the die, but would not cover the package periphery to allow for the exposure of the top lands that were required for interconnecting the top and bottom PoP. This design would lead into a thicker overall stacked package height due to the molding requirement for the bottom PoP. Also, the wire bonded design would require additional space around the die for wire bond pads. The space required for bonding pads would essentially limit the maximum die size that could be designed into these packages without increasing the package body size.

The introduction and use of the flip-chip (FC) provided two main advantages over the traditional wire-bond designs in terms of the max allowed die size and the package height. With flip chip, the encapsulation of the die was no longer needed, which resulted in lower package height, and the elimination of the wire bond pads freed the space on package to allow for larger die size. Other variants of PoP proliferated to meet the package warpage requirements and to further provide a path to tighter pitch at top lands for memory interface. The following paragraphs describe and compare these package types.

Bare-die PoP has the simplest process flow compared to all other PoP package configurations, and provides the lowest cost option among all PoP package types. High level process flow includes die prep, Flip-Chip (FC) attach/ reflow, followed by Underfill (UF) process, bottom BGA solder ball

attach, and singulation. This is the same as the process flow for a typical FCFBGA type package.

Plasma process is usually incorporated prior to UF dispense process in order to enhance the UF capillary flow, and to eliminate UF voids that could lead to reliability issues. The presence of the top lands on bottom PoP package present additional challenges for the UF process as the UF fillet must be tightly controlled in order to avoid pad contamination. Resin bleed that is also associated with some UF materials, especially those with Amine base, pose additional risk with respect to top land pads contamination and must be controlled. To address this resin bleed issue Solder Resist Dam is applied adjacent to the inner row of top lands to contain the bleed and hence prevent the pad contamination. Figure-1 shows the typical UF fillet and standard deviation for a typical package with the application of SR Dam.



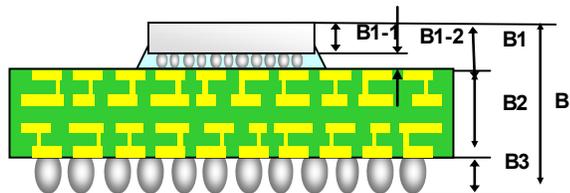
Die Side	Std Dev (mm)
A	0.03
B	0.02
C	0.01
D	0.02

Figure-1: Underfill standard deviation (mm)

In order to minimize the package height, the flip-chip die is usually thinned down to 100 micron (um), and substrate thickness is reduced to as thin as possible while meeting the package warpage requirements. Current technology allows for 0.4mm bottom BGA pitch and 0.5mm top pad pitch. Figure-2 shows the stack up analysis for a bottom PoP package using a 100um thin die and a 430um thick 4 layer laminate substrate, and Figure-3 shows the actual cross section of this package.

The maximum package height is 0.854mm including the 250um BGA ball size. After stacking with top PoP (memory module package) with 3 stacked die configuration, the total stacked height is around 1.45 mm. Depending on the substrate and core thickness used, this package can meet the max height of less than 0.8mm. High temperature warpage performance of this package is the key to a successful and high yield stacking process that is required for joining the top and bottom PoP together during the reflow process [1]. Typically, Surface Mount (SMT) board manufacturers require 60 to

80um warpage at above solder liquidus temperature of 220 C up to peak reflow temperature of 250~260C. Figure-4 shows the typical thermo moiré warpage performance of this package based on a set of Underfill materials. JEDEC warpage sign convention is used to show the warpage of the package in which positive warpage is shown as frown or convex warpage shape with BGA balls facing down [2].



Items	Symbol	Nom	Remark
Die thickness + Collapsed bump height	B1	0.195	
Die thickness	B1-1	0.100	Die thickness tolerance +/- 12.5um
Collapsed bump height	B1-2	0.095	Original bump height = 90um SOP height = 30um
Substrate thickness	B2	0.450	core thickness = 200um ??? Substrate thickness copied from Hera
Stand-off	B3	0.210	0.300mm solder ball on 275-280um SRO, 0.500 mmpitch
Bottom PKG height	B	0.855	

Figure-2: Bare-Die PoP stack up analysis



Figure-3: Bare-Die PoP package cross section

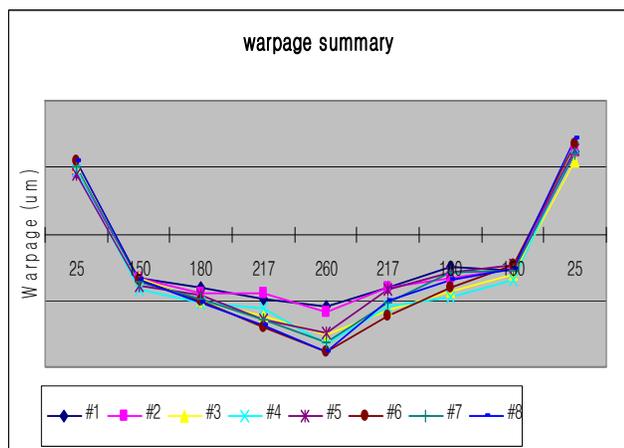


Figure-4: Package high temperature warpage performance vs. UF material type

65nm Si with eutectic SnPb bumps are in production and 40/45nm Si with lead-free bumps are being introduced. Top lands are usually NiAu plated and bottom lands have Cu-OSP (Organic Solder Preservative on Copper). With the introduction of 45nm Si with Extra Low-K dielectric (ELK) layers and the use of Lead-Free SnAg solder bumps, issues such as Inter Layer Dielectric (ILD) crack and bump cracks

have had to be resolved in order to pass the package level reliability requirements. Early on in development stage it was realized that the changes to materials and processes had to be done on both FAB and assembly level. As a result of joint development projects between the assembly and wafer FAB key changes to FAB back-end and bumping process were made to resolve the ILD crack issue. These changes to the bumping process along with optimization of the UF material in assembly were the key in elimination of White Bumps (WB) or ILD crack that were observed post UF cure process and through the subsequent temperature cycle reliability evaluations. Based on these changes, bare-die PoP in 45nm and with lead-free solder has successfully passed all component level reliability tests including JEDEC Level-3 moisture sensitivity, Temp cycle condition-B, 1000 cycles, Highly-Accelerated Temperature and Humidity Stress Test (HAST) 192 hrs, and 1000 hrs High Temp Storage (HTS) [3, 4, 5].

Embedded Solder On Pad (eSOP) is another version of PoP package and it is referred to as eSOP-PoP. Due to the encapsulation molding process, this package can be either in flip-chip or wire-bond format. The over-mold structure on this package also provides the advantage of better warpage performance, in addition to providing better die protection. This package will undergo several reflow steps throughout the assembly process as it requires the top pad solder ball attach and reflow prior to die attach or FC attach process. Package warpage is controlled not only by the choice of the substrate core type and thickness, but also by the choice of the molding compound. Figure-5 shows the high temp package warpage behavior as a function different mold compounds.

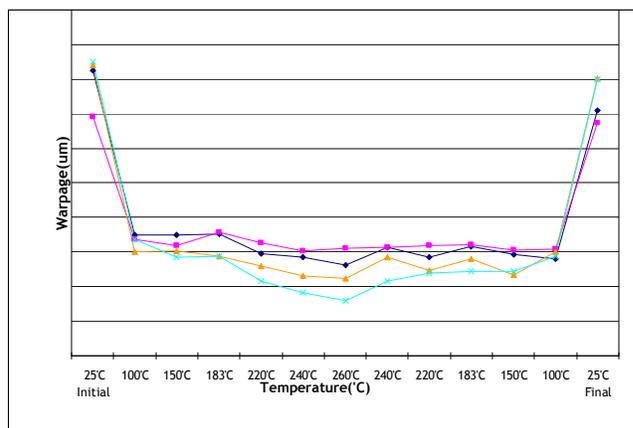


Figure-5: eSOP-PoP high temp package warpage vs. EMC material type

One of the critical steps in the process flow of this package is the half-cut process step where the mold compound on the top periphery of the package is cut in order to expose the embedded solder balls.

Laser-Via PoP is another form of PoP. Similar to the eSOP-PoP this package has molding encapsulation that protects the die and provides better warpage performance as compared to the bare-die PoP.

This package uses laser ablation for drilling the holes through the molding to expose the top solder balls. As such, laser ablation is one of the critical process steps in this package to control the uniformity of the formed vias. The via quality is defined by the Outside Hole Diameter (OHD), Inside Hole Diameter (IHD), and via depth, which is measured from the top mold surface to top of solder balls, Figure-6

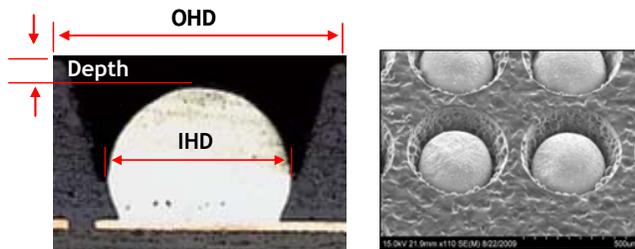


Figure-6: Laser Ablation and laser via critical dimensions

The metrics used to optimize these critical dimensions include the package-to-package spacing/ gap, solder joint profile, total stacked package height, and Open/Short test for verification of electrical continuity between the top and bottom package. Figure-7 shows the cross section of the stacked package with top memory module attached to the bottom PoP and mounted on the PCB.

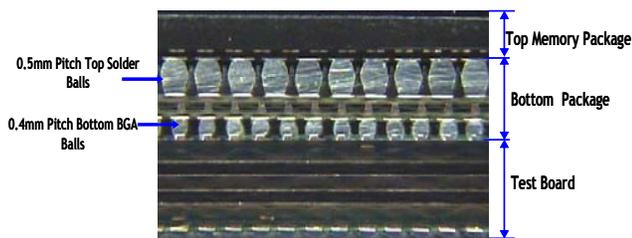


Figure-7: Cross section of MLP package with top memory module mounted

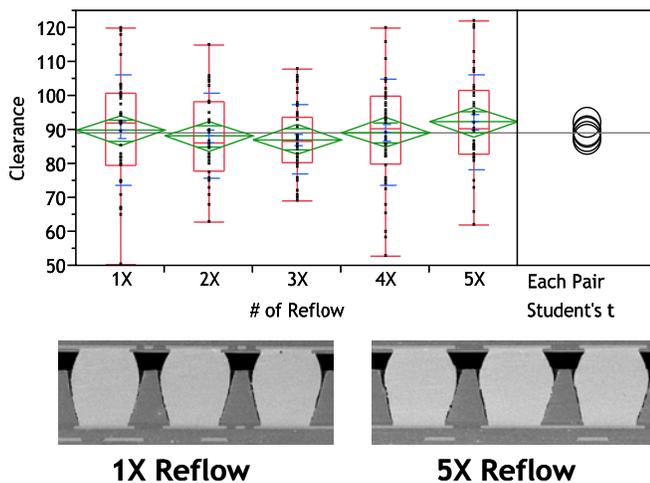


Figure-8: Package-to-Package gap based and solder joint shape vs. number of reflows

This package has 0.5mm top ball pitch and 0.4mm bottom BGA pitch. Figure-8 shows how the optimum process window is validated for the critical parameters by examining the package-to-package spacing, and total package height. In this study, all the 560 units including all the process corner conditions that were stacked successfully passed the open/short test.

This package uses advanced assembly processes including 150um bump pitch flip chip process with 45nm node Si, and aggressive UF process and materials to control the UF spread and Keep Out Zone (KOZ) to less than 1mm on the dispense side with high Cpk values. As a result, die size as large as 9x9 mm squared can be placed in a 14x14mm package that has 3 rows of top lands on bottom PoP package (see Figure-9)

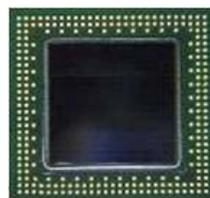


Figure-9: 14x14mm MLP PoP with 9x9mm die size

The use of molding that encloses the top balls provides additional mechanical support between the top and bottom package after the stacking process, which can help improve the drop-test and BLR performance. The proper choice of the mold compound by optimizing the glass transition temperature (Tg), modulus, and shrinkage of the mold compound will also affect the warpage performance.

### Next Generation PoP and 0.4mm Top Pad Pitch

The difference among PoP package types can be seen by examining the package requirements for enabling the 0.4mm top ball pitch. The main drivers for this top pad pitch reduction is to increase interconnect density, free the additional space that would have otherwise been taken by the top pads in package periphery, and reduce package size. This freed space can be used to allow for a larger die size in the same package footprint. In addition to providing more room for accommodating a larger die size, this pitch reduction will also result in a lower total stacked package height as smaller ball size would have to be used in conjunction with the smaller pitch. The following figure shows the maximum stacked package height and the resulting flip-chip die thickness for both 0.5mm and 0.4mm top pad pitch for all three PoP configurations.

While from the design standpoint this top pad pitch reduction can be implemented in each of the PoP package types, the above graph shows that in practice bare-die PoP and eSOP-PoP have more limitations in terms of the die thickness reduction that prevent the utilization of this pitch reduction on these two package types. On the other hand, given the laser via exposure of top balls, Laser-Via PoP package enables the top pad pitch reduction more easily compared to the bare-die PoP and eSOP-PoP package.

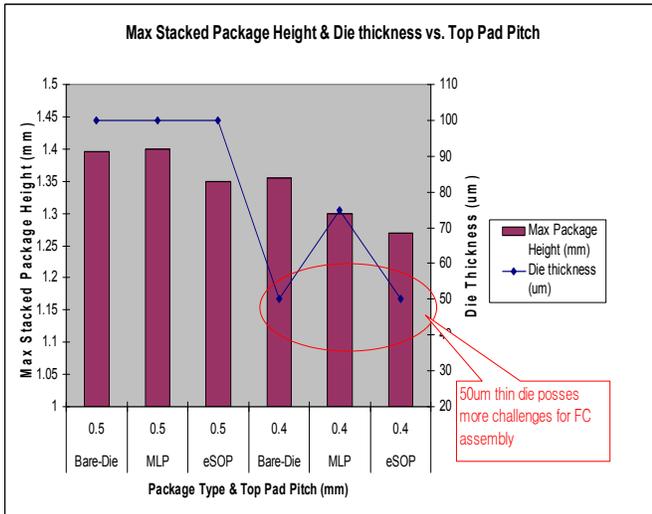


Figure-10: Max stacked package height & die size trends vs. package configuration & top ball pitch

This die size reduction is driven by the physical interference that would result between the top and bottom package due to the pitch reduction and the resulting decreased collapse height. In this regard, Laser-Via PoP is more forgiving and allows for a larger package-to-package spacing compared to bare-die and eSOP PoP. As a result, for Laser-Via PoP a thicker die can be used relative to the other two package types. This package to package spacing for the three different PoP packages is shown in figure 11, for both 0.5mm and 0.4mm top ball pitch.

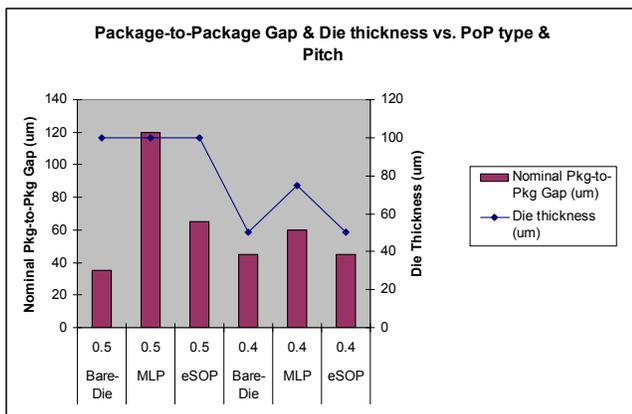


Figure-11: Package-to-Package Gap & Die thickness vs. package configuration & top pad pitch

In addition, there are a number of different modulators that can be used to lower the overall stacked package height such as substrate thickness reduction, BGA ball size reduction, and mold cap reduction. Changes to each of these variables have their own implications and tradeoffs. For example, change in the substrate thickness could affect the package warpage performance, and change in the ball size could affect the SMT reliability. The following figure predicts the overall stacked package height for various PoP configurations with 0.4mm top ball pitch.

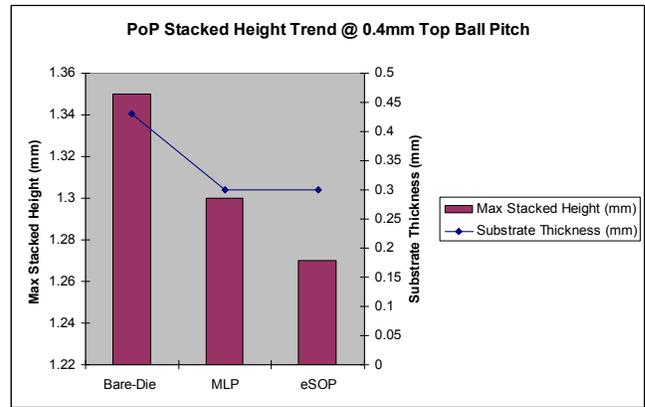


Figure-12: Max package stacked height for 0.4mm top ball pitch

Additional package height reduction can be realized by the use of ultra low CTE core substrate materials and thinner mold compounds as long as the overall package warpage spec limit are met. These will be the areas of focus and development for the next generation of PoP package.

Further integration and form factor reduction for PoP can be achieved by the use of Embedded Wafer Level Ball Grid Array (eWLB), which is a Fan-Out Wafer Level Package and has been established as a joint industrial initiative between STATSChipPAC, ST Ericsson, and Infineon. This package allows for wafer level packaging of the logic die through redistribution of bump pads and eliminates the costly laminate build-up substrates that are typically used in PoP packages. The Fan-Out/ Fan-In redistribution structure allows for reduction of package foot-print as well as the package height reduction, whereby a 12x12mm package can have height of 0.5mm. The Fan-Out (FO) approach allows for higher IO count in a smaller package size that leads to higher IO density. The reduced interconnect lengths will also provide better electrical performance and lower parasitic that are associated with long interconnect paths. The reconstituted wafer can have isolation and metal layers on both sides and be electrically connected by the means of conductive vias. As a result, top side pads are used to provide the interconnection to the memory package BGA balls, and bottom pads are used for connection of package to the Printed Circuit Board (PCB).

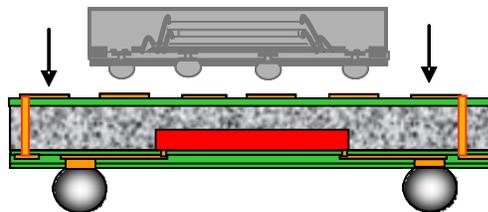


Figure-13: eWLB, PoP configuration

## Conclusions

PoP packages have proliferated from the conventional wire-bond over-molded design to bare-die flip-chip PoP and further to Embedded-Solder-On-Pad (eSOP) PoP and Laser-Via PoP. All of these packages are available for production. The current HVM process is capable of providing 0.4mm bottom BGA pitch and 0.5mm top ball pitch for memory interface, and advanced ELK FAB nodes and lead-free bumps are ready for production. Challenges with respect to ILD crack and bump crack associated with 45nm ELK Si and SnAg lead-free solder have been overcome by optimization of bumping process and assembly processes and materials. While eSOP PoP can provide the lowest stacked package height among all the various PoP package configurations, Laser-Via PoP seems to be the most promising option going forward with transition to 0.4mm top ball pitch based on the relatively more relaxed requirements for die thickness. Bare-die PoP and eSOP PoP have more challenges in meeting the 0.4mm top pad pitch requirement due to package to package interference, which necessitates the use of even a thinner flip-chip die compared to Laser-Via PoP. However, bare-die PoP has the lowest cost structure and risks of die thickness concerns can be resolved.

## Acknowledgments

This work and paper could not have been completed without the efforts of the engineering managers and engineering staff members of STATS ChipPAC Research and Development (R&D) group in Korea under the guidance of Kenny Lee as head of worldwide R&D, and contributions from Flynn Carson, VP of technology marketing.

## References

1. Vijayaragavan, N., Carson, F., Mistri, A., "Package on Package Warpage – Impact on Surface Mount Yields and Board Level Reliability", Proc of 58<sup>th</sup> IEEE ECTC, Lake Buena Vista, FL, May 2008, pp 389-396
2. JEDEC, " High Temperature Package Warpage Measurement Methodology", JESD22-B112, May 2005
3. JESD22-A104D; Temperature Cycling, May 2005
4. J-STD-020D.1; Moisture/Reflow Sensitivity Classification, March 2008
5. JESD22-A110-B; Highly-Accelerated Temperature and Humidity Stress Test. Feb. 1999
6. JESD22-A103C; High Temperature Storage Life test, Nov 2004.