Low Cost Cu Column fcPoP Technology

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Abstract

Package-On-Package (PoP) is now a wide-spread 3D package technology used in Smartphones, TABLET devices, and in some Gaming applications. The vertical integration of high speed memory packages such as DDR-II and form factor reduction are the main drivers for adoption of these package types. Continuous trends in bump pitch reduction and performance improvement in combination with higher density Si have created the need for Cu column design for Flip Chip bumps. Also, adoption of Cu column and the associated Bond-on-Lead (BoL) technology provide substrate cost reduction through design rule relaxation, which is key for cost sensitive PoP packages and consumer electronics, in general. In this paper a 65nm Si originally designed with wire bond pads is converted to Flip Chip using the Bond-on-Lead (BoL) interconnect structure. Cu column height and solder cap volume are optimized to allow for uniform wetting of bump to substrate trace while also providing the required gap height needed for proper Capillary Underfill (CUF) process, which otherwise would have not been possible by using the solder bumps at such a given tight bump pitch. Center grid bump array at 250um bump pitch was added to the original design in order to provide mechanical support for the Flip-Chip-attached die and also to promote the CUF process. Polyimide re-passivation was used prior to bumping process in order to enable a Cu bump structure with suitable design rules for assembly with the additional benefit of providing Low-K dielectric protection. The CUF process was successfully developed for sub-50um stand-off height to meet the void-free process requirement. Package type is a12x12mm bare-die fcPoP configuration with 6 layer Build-Up (BU) and top and bottom ball pitch of 0.5mm and 0.4mm, respectively. All functional tests and package level reliability including Moisture Sensitivity Level-3 (MSL3), Temperature Cycle-B (TC-B) 500 cycles, High Temperature Storage (HTS) 500 hours, and unbiased HAST 96 hours were successfully passed. Board Level Reliability (BLR) tests including Drop Shock and Temperature Cycle were completed and successfully passed with the first failure in drop test occurring at 152 cycles, and no failures up through 1000 cycles of temperature cycle.

1. Introduction

Adoption of Cu column in place of flip chip solder bumps has number of potential benefits including bump pitch reduction, possible design rule relaxation by using wider Line and Space for signal routing in a given design, removal of part of fcCuBE™ process that provides a low cost flip chip solution set. In addition to the benefits achieved by BoL design as described above, other components of this technology include MUF that provide additional assembly cost reduction for package types where applicable [1], [3].

tight Solder Resist Opening (SRO) tolerances, and the removal of Solder-On-Pad (SOP), all of which result in a low cost flip-chip package solution. The reduction in pitch capability is simply driven by the fact that bump to bump spacing can be controlled better with Cu column as compared to solder bump due to the bump geometry, spherical for solder vs. cylindrical for Cu, in addition to the differences that exist in the bump geometry post reflow process. In post reflow, solder tends to collapse and an increase in bump diameter is observed, whereas Cu column will not go through such transformation and any dimensional changes. Furthermore the collapse height, which defines the die to substrate gap (stand-off height), can be better controlled by Cu column as the column height can be modulated to provide the required stand-off height without any increase in bump diameter, whereas for solder bump, any increase in stand-off height is associated with the increase in bump diameter. Such increase in bump diameter is not desirable as it would reduce the bump to bump spacing and hence result in potential bump bridging and electrical shorts. Additionally, the reduced bump to bump spacing would create issues for Capillary Underfill (CUF) flow and lead in to UF voids. Alternatively, it would create the similar UF voiding problem for the Molded Underfill (MUF) process [1].

Due to the tight bump pitch capability achieved by Cu column process, existing wire bond design with fine pitch peripheral bond pads can easily be converted to Flip-Chip (FC) design without the need for RDL (Redistribution Layer) that would otherwise be required for fanning-in the tight pitch peripheral wire bond pads to a coarser inner FC bump array. For conventional flip-chip solder bumps the substrate pads with SOP are Solder Mask Defined (SMD) and Solder Resist Registration (SRR) and Cu pad dimensions on substrate result in a very narrow space in between the substrate pads for any escape routing. The SMD pads are required in order to contain the solder from wicking down the trace. As a result, any such escape traces will have to use finner line width and trace to trace space, which result in substrate cost adders. However, through the use of Cu column solder volume is controlled to the finite amount deposited on the Cu column, and hence the SMD substrate pads are no longer required. Through the elimination of SMD pads and the SOP, the bond pads are converted to narrow bond traces and furthermore Solder Resist (SR) can be removed as it is no longer needed to confine the solder wicking, hence resulting in substrate cost reduction [2]. The resulting BoL structure is an integral

2. Test Vehicle Description

In the existing package, the original 65nm node Si was designed with peripheral wire bond pads at 94um bump pitch. Due to the electrical performance issues associated with long wire loops it was desired to convert the chip to flip-chip
design without the use of RDL in order to avoid the redistribution cost adder in the bumping process. Figure-2.1 below shows the schematic of the peripheral Aluminum (Al) metalized wire bond pads and the location of vias that were later formed through the Polyimide (PI) re-passivation process resulting in the same 94um bump pitch.

However, the conversion to flip-chip design in this configuration would leave the center area of the chip completely bump-free, which would raise concerns for the Capillary Underfill (CUF) process in addition to the lack of any mechanical support that would have been provided by presence of any flip-chip joints in area array format. As a result, it was decided to populate the area enclosed by the peripheral bumps with an array of bumps that would only serve as mechanical joints to provide the mechanical integrity that would be needed to pass the reliability requirements. In addition, the center bump array fills the large void under the die that would have been difficult to fill with UF in a void-free manner due to the lack of capillary force. Figure-2.2 below shows the overall bump layout after the inclusion of the center bump array.

Bumping process included PI re-passivation, lithography, Under Bump Metallization (UBM), and Cu column plating with a SnAg solder cap on top. As a result of this bumping structure, the peripheral bumps were located on the Al pads while the center mechanical bump array was located on the top passivation. Figure-2.3 below shows the Cu bump and Lead-Free (LF) SnAg solder cap along with UBM & PI passivation structure that were formed through the bumping process. For the given 94um peripheral bump pitch, Cu column diameter of 60um was plated, followed by Ni barrier metal and the top solder cap. Overall Cu column and solder cap height were optimized in order to create the minimum stand-off height required for successful CUF process.

Figure-2.3, Peripheral array Cu bump and LF solder cap dimensions

Figure-2.4 below shows the center array bump structure that is sitting directly on the top SiN passivation.

Substrate design on top M1 metal layer consisted of narrow bond traces for the peripheral pads and SMD type pads for the center bump array as shown in Figure-2.5 below. The peripheral bond pads with trace design require no SR and hence the entire SR within this area is removed.

Figure-2.5, Substrate pad design, center array SMD pads (left) and BoL (right)

The peripheral BoL design and center array SMD pad design are shown in Fig.2.6 below.
Package configuration in this evaluation as shown below (Fig. 2.7) was Package-On-Package (PoP) in bare die format known as fcPoP, 12x12mm body size, 0.4mm bottom Ball Grid Array (BGA) pitch, 0.5mm top pad memory interface pitch, in 6 layer Prepreg (PPG) Build-Up (BU) design, and with Si die thinned down to 100um thickness. Substrate core material was chosen as Ultra Low CTE (UL CTE) material to control the high temperature warpage and room temperature co-planarity of the package, which is a key performance metric for PoP package types due to its effect on the stacking yield. Substrate top PoP pads (memory interface pads) were electrolytic NiAu plating, and the bottom BGA pads were Cu OSP surface finish. Figure 7 below shows the bottom PoP package, known as bare die fcPoP, along with the top memory package in the pre-stacked configuration. Together with the top package stacked on bottom package, the maximum height of the pre-stacked PoP is measured at 1.54mm, which is due to the thick 6 layer substrate that is being used in this design. Other fcPoP packages in production today are measured to as high as 1.3mm with 4 layer PPG BU substrates, and these package are predominantly used in mobile application space. Bare die fcPoP is the lowest cost PoP solution amongst the portfolio of PoP packages as it has the simplest process flow. This package type as with other PoP package types are used in mobile application space, particularly in Smartphones, where 3D integration and low profile packages are required [3]. Bare Die fcPoP has long been qualified and in production with solder bump, however, the integration with BoL and fcCuBE™ had not yet been achieved.

3. Assembly Process Characterization

The Assembly process characterization consisted of Chip Attach (CA) process setup, UF material selection and process optimization, and Ball Grid Array (BGA) attach. The main process monitors used in process setup included X-ray for CA non-wets, UF CSAM for UF voids, and Inner Layer Dielectric (ILD) CSAM for ILD cracks or White Bumps (WB). CA process consisted of applying the suitable flux and reflow profile for the formation of solder joint between the Cu column with LF SnAg cap and the substrate pads with Cu OSP surface finish. Given the bump design and substrate bond pad configuration, two different joint geometries were resulted as shown in Fig. 3.1 below, for center array SMD pads, and the peripheral array BoL pads. Prior characterizations on 65nm Low-K and lower Si nodes with ELK (Extra Low K- Dielectric) have shown the BoL structure as being more robust with respect to ILD crack protection vs. the comparable SMD joint configuration shown above. These findings have been proven by empirical data as well as the Finite Element Modeling (FEM) and have been reported extensively in prior papers [4], [5].

As a result, in the given design, peripheral bump pads that were the functional bumps and designed in BoL configuration provided the ILD crack protection and no cracks or White Bumps (WB) were observed through assembly characterization and reliability tests including Temperature Cycle (TC), condition B as reported later in this paper. The center array bumps had no impact on ILD crack since they had no electrical connectivity and were designed for mechanical integrity as described earlier. Further process characterization and the subsequent large sample verification builds proved the CA process yield with respect to bump bridge and non-wets to be very robust and manufacturing capable.

UF process characterization focused on void-free UF process and control of UF creep on die in addition to UF bleed. UF bleed is especially critical for PoP packages as any resin bleed onto the top PoP pads (memory interface pads) will cause pad contamination that will render the subsequent stacking process problematic with non-wets and yield fall-outs. In this application UF process optimization was very challenging due to the Cu column diameter and height that were used. Cu column height, and solder cap height are both the function of Cu column diameter and as the diameter decreases, the resulting column height and solder cap volume that can be plated decrease. This will result in a lower die stand-off height post CA reflow and bump collapse that is expected. In this particular design with 60um Cu column diameter as was described earlier, die stand-off height measures at about 35um nominal as shown in Fig.3.2 below.
The peripheral bumps show a higher stand-off height due to the open SR design that is used for peripheral pads, while the center array SMD pads sow a lower stand-off height due to the presence of SR on substrate. UF process must be optimized properly to fill the area under the die with this varying gap height void-free. Figure-3.3 below shows the matrix of various UF materials used in this evaluation in conjunction with plasma vs. no-plasma before the UF process.

Figure-3.3, UF materials used for UF process optimization

UF fillet measurement for the various materials studied showed high Cpk (process capability) with respect to the fillet specification for assembly process, as shown in Fig-3.4 below.

![Figure-3.3, UF materials used for UF process optimization](image)

Figure-3.4, UF material fillet measurements

However, the UF creep on die performance as shown in Figure-3.5 below shows some variation and material A exhibits the best performance with respect to creep on die as well as having high Cpk for fillet measurement and void-free results. This material also has also been extensively proven in various LF device applications and has passed numerous package reliability tests for Si nodes down to 28nm. As a result, material A was chosen as the UF material for this product.

![Figure-3.4, UF material fillet measurements](image)

Figure-3.5, UF creep on die performance

Another key quality metric for PoP package is the Thermo moiré or high temperature warpage performance of the package, which is critical in ensuring optimal stacking yield. Typically, the high temperature warpage, as measured on the BGA side of the substrate, has a spec limit of 80um. Figure-3.6 below shows the Thermo moiré warpage plot of this package for the various UF compounds that were evaluated above.

![Figure-3.6, Thermo moiré warpage performance vs. UF types](image)

Material type-A meets the warpage spec of 80um as shown above plot.

Through the package level reliability testing it became clear that the UBM and PI passivation opening needed to be redesigned in order to fix the Open failures that were seen post Thermal Cycle, condition B (TCB) testing. Failures were detected post 500 cycles TCB and the Failure Analysis (FA) work confirmed the root cause of the open failures as the delamination between the UBM and the underneath Al pad, as defined within the top PI passivation opening. This delamination was due to the high stresses exerted on the bump structure during the TCB cycles and the small adhesion contact area that was defined by PI opening. As a result, UBM dimension was increased along with the bump diameter in order to increase the PI opening area. Side-by-side reliability testing of the two different UBM size and PI opening were carried out and results clearly verified the root cause as the PI opening design. Figure-3.7 below shows the validation reliability results that show the improvement gained by enlarging the PI opening.

![Figure-3.7, Effect of PI opening on UBM delamination and TCB open failures](image)

The subsequent package reliability tests were fully passed and met the product requirements, which were; Moisture Sensitivity Level 3 (MSL3), TCB 500 cycles, unbiased HAST 96 hours, and 500 hours High Temperature Storage (HTS) test.
4. **Board Level Reliability Tests**

An eight layer JEDEC Drop Test (DT) board was designed seating fifteen units. Top memory and bottom PoP package were stacked and reflowed on to the DT board in reflow oven using SAC1205 solder, forming simultaneously the joints between the top and bottom package and on to the test board. Four separate chains were designed to monitor the solder joints during the drop test. One chain for the bottom corner BGA balls to DT board, one chain for center BGA array to the drop test board, one chain for monitoring the Cu column/FC bumps connection to the substrate, and one chain for connection between the top memory and bottom logic package. Total of three DT boards and 30 units were used for DT evaluation and Weibull plot generation per JEDEC spec of 1500G acceleration and pulse duration of 0.5mSec. Figure-4.1 below includes schematically the package configuration for drop test, the summary table of DT failures, and the Weibull plot. As can be seen, the first failure occurred post 152 drop cycles, easily meeting the minimum 30 cycles required. Additionally, all failures were identified at the interface between the bottom BGA balls and the drop test board, none for the flip chip bumps and none between the top and bottom connections.

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**Figure-4.1, JEDEC Drop Test results of the stacked package configuration**

Board Level Reliability (BLR) Temperature Cycle (TC) was done using total of three TC boards and eighteen units with SAC1205 up to 1000 cycles at -40~125 C. As in the DT board design, total of four chains were used for detecting the open failures through the TC process. Test read points were at T0, 500 cycle, and 1000 cycles. All samples passed 1000 TC without any failures. Figure-4.2 below shows the x-section BGA solder joints for failed DT samples, good DT samples, and good TC samples.

**Figure-4.2, BLR DT and TC Units**

5. **Conclusions**

Cu column and BoL enables the reduction of flip chip bump pitch beyond what can be achieved with solder bump. Alternatively, for the same bump pitch as with solder bump design, larger bump to bump spacing is created, which can result in more relaxed line and space design rule on substrate. In combination with elimination of SOP and open SR design rules, these changes result in a lower cost package. The technology can also be used for conversion of wire bond designs into flip chip without the use of RDL, which would be a cost adder in bumping process. In this paper, a sub-100um pitch wire bond design was converted into flip chip through the implementation of Cu column and BoL trace design, which enabled the product transformation from wire bond to flip chip at a low cost while improving the performance requirements that were needed for the end application. Cu column height was designed to provide the stand-off height required for void-free CUF process and it was proven that the conventional CA process with mass-reflow can be used successfully for sub-100um bump pitch applications. Package type used in this application was fCfPoP and package qualification passed MSL3, 500 cycles TC, condition B, 96 hrs uHAST, and 500 hours HTS. BLR tests including drop test and TC were performed on JEDEC test board. First failure in DT occurred at 152 cycles of drop, and 1000 cycles of TC (~40~125C) were completed successfully without any failures.

6. **Acknowledgments**

The entire development and process characterization work reported in this paper were the result of engineering work done at STATSChipPAC Korea flips chip R&D team. Additionally, Ty Chen from STATSChipPAC Taiwan wafer bumping R&D had major contributions in development and qualification of the Cu bumping process.

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