“300mm Large Scale eWLB (embedded Wafer Level BGA): Cost Effective Solution with Performance”

by

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Demand for Wafer Level Package (WLP) is being driven by the need to shrink package size and height, simplify the supply chain and provide a lower overall cost by using the infrastructure of a batch process. The increasing demand for new and more advanced electronic products with smaller form factor, superior functionality and performance is driving the integration of functionality into the third dimension. There are some restrictions in possible applications for fan-in WLPs since global chip trends tend toward smaller chip areas with an increasing number of interconnects. The shrinkage of the pitches and pads at the chip to package interface is happening much faster than the shrinkage at the package to board interface. This interconnection gap requires fan-out packaging, where the package size is larger than the chip size in order to provide a sufficient area to accommodate the 2nd level interconnects. eWLB is a type of fan-out WLP that has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology. 200mm eWLB is in HVM from industry last three years and there was need to move 300mm for scaling-up and low-cost solutions. eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. Alongside, there are physical constraints such as its footprint and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency).

A. Challenge of 300mm large scale eWLB

For 300mm eWLB, there is area increase of more than 230% compared to 200mm as shown in Figure 1. So warpage is most critical for larger scale wafer handling as like in wafer fabrication process. Warpage affects wafer handling, processability, throughput as well as process stability thus yield so it is critical to optimize and well control its warpage behavior. Figure 2 shows clearly warpage difference between 200mm and 300mm eWLB wafers. With computational simulation work for 300mm eWLB, it showed more than 2 time warpage than 200mm case.

To optimize these warpage behaviors, various material/process parameters were studied. After basic thermal-mechanical simulation study of these parameters with several DOE (Design of experiment), key parameters were identified such as dielectric materials and thickness, molding compound thickness etc. Based on those parameters, in-depth simulation was carried out for several combinations of each parameters. Figure 2 showed the warpage behavior with different materials sets. With different set of materials, it showed significant warpage behaviors with maximum difference of 1000um (1mm).
Fig. 2 Computational mechanical warpage simulation data with (a) 200mm (max. 770um) and (b) 300 mm eWLB (max. 1846um)

B. Component level and Board level reliability test result

For 300mm eWLB package’s reliability tests, test vehicle were prepared with 8x8mm and 183balls with 5x5mm die size. JEDEC standard reliability tests were carried and eWLB passed all reliability conditions. For board level reliability, JEDEC TCoB (temperature cycle on board) and drop test were carried out and it also successfully passed all test requirements as shown in Table 1.

Table 1. Summary of eWLB Component level and Board level reliability test result

<table>
<thead>
<tr>
<th>Moisture Sensitivity Level</th>
<th>Temperature Cycling</th>
<th>High Temperature Storage</th>
<th>Unbiased HAST</th>
<th>Temperature Humidity Bias Test</th>
<th>TC on Board</th>
<th>Multiple Solder Reflow</th>
<th>Drop Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL1 @ lead free condition (260°C)</td>
<td>-40°C/125°C, 850 cycles</td>
<td>150°C, 1000 hrs</td>
<td>130°C/85% RH, 96 hrs</td>
<td>85°C/85%/6V, passed 1000 hrs</td>
<td>-40°C/125°C, 2 cycles/hr, passed 500 cycles</td>
<td>5x, 10x and 20x refloows with minimal reduction in bump shear strength</td>
<td>Passed JEDEC drop test for 8 x 8mm, 183 balls (0.5mm pitch)</td>
</tr>
</tbody>
</table>
C. Summary and future works

Advanced packaging plays a crucial role in driving products with increased performance, low power, lower cost and smaller form factor. The industry requires innovation in packaging technology and manufacturing to meet current demands and the ability to operate equipment in high volume with large throughput. eWLB technology is an enhancement to standard WLPs, allowing the next generation of a WLP platform due to its fan-out capability.

eWLB is a low-cost solution with batch process and larger area utilization such as 12” and panel approaches. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SiP) and 3D stacked packaging. Moreover, 3D eWLB technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of devices as well as 3D TSV integration for true 3D SiP systems. For further cost reduction approach after 300mm eWLB, scaling-up such as panel approach would be next steps to move. It provides breakthrough productivity, compatible process for advanced Si node devices as well as functional Integration /combination of different node devices (32nm, 28nm or 22nm) with RF, discrete or memory devices.