“Electrical, Thermal and Mechanical Characterization of eWLB (Embedded Wafer Level BGA)”

by

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ABSTRACT
Demand for WLP (Wafer Level Package) is being driven by the need to shrink package size and height, simplify the supply chain and provide a lower overall cost by using the infrastructure of a batch process. WLP is the upcoming future packaging technology. The increasing demand for new and more advanced electronic products with smaller form factor and superior functionality and performance, is driving the integration of functionality into the third dimension. There are some restrictions in possible applications for fan-in WLPs since global chip trends tend toward smaller chip areas with an increasing number of interconnects. The shrinkage of the pitches and pads at the chip to package interface is happening much faster than the shrinkage at the package to board interface. This interconnection gap requires fan-out packaging, where the package size is larger than the chip size in order to provide a sufficient area to accommodate the 2nd level interconnects. eWLB is a type of fan-out WLP that has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology.

This paper will highlight some of the recent characterization works of electrical, thermal and mechanical performance of eWLB packaging. The performance compared with other packaging format, ie. FI-WLP (Fan In-WLP) and fcBGA (flipchip Ball Grid Array) packages is discussed. Thermal resistance, $\theta_{ja}$ of eWLB packaging is studied and it is found comparable with those of FI-WLP and fcBGA. Thermal characterization activity is carried out to investigate the effect on eWLB configuration with power loading. Thin film based integrated passives on the fan-out area (mold material) of the eWLB is also analyzed during RF performance characterization. Due to the low-loss property of the mold material, plated Cu inductors showed high quality-factor (Q) performance. The mold material in fan-out area is not only used as a supporting substrate, but also serves as the package substrate, which allows the high-Q inductors to be implemented with other RF chips in one single package. Parasitic electrical performance and characterization works will be presented in this paper. eWLB package warpage behavior with temperature profile observed with Thermo-Moire method result will be presented in this paper too.

INTRODUCTION
WLP applications are expanding into new areas and are segmenting based on I/O count and device. The foundation of passive, discrete, RF and memory device is expanding to logic ICs and MEMS. The WLP segment has matured over the past decade, with numerous sources delivering high-volume applications across multiple wafer diameters and expanding into various end-market products. With infrastructure and high volumes in place, a major focus area is cost reduction.

One of the most well known examples of a FO-WLP structure is eWLB technology [1]. This technology uses a combination of front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer, which can greatly reduce manufacturing costs. Its benefits include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count, maximum connection density, as well as desirable electrical and thermal performance. It also offers a high-performance, power-efficient solution for the wireless market[2]. Furthermore, next generation 3D eWLB technology enables 3D IC and 3D SiP (System-in-Package) with vertical interconnection. 3D eWLB can be implemented with through silicon via (TSV) applications as well as discrete component embedding.

eWLB TECHNOLOGY
eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. Alongside, there are physical constraints such as its footprint and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency).

The obvious solution to the challenges was some form of WLP. But two choices presented themselves: Fan-out or Fan-in. FO-WLP is an interconnection system processed directly on the wafer and compatible with motherboard technology pitch requirements. It combines conventional front- and back-end manufacturing techniques, with parallel processing of all chips. There are three stages in
the process. Additional fab steps create an interconnection system on each die, with a footprint smaller than the die. Solder balls are then applied and parallel testing is performed on the wafer. Finally, wafers are sawn into individual units, which are used directly on the motherboard without the need for interposers or underfill.

Figure 1. (a) eWLB wafer after packaging with reconstitution, RDL and backend processes. (b) eWLB package after singulation.

Figure 2. SEM micrographs of cross-section of eWLB[1].

Advantage of eWLB Technology
The current BGA package technology is limited by the organic substrate capability. Moving to eWLB helps overcome such limitations and also simplifies the supply chain. Building the substrate on the package itself allows for higher integration and routing density in less metal layers. eWLB is a next generation platform that will support future integration, particularly for wireless devices and this packaging technology has a number of important features. Transition to eWLB packaging technology enables a significant reduction in recurring costs by eliminating the need for expensive substrates. The advantage of eWLB packaging can be summarized in Table 1. BGA packaging also faces a challenge with technology nodes beyond 65nm as the device performance density drives the need for flip chip. But advanced flip chip nodes drive fine pitch combined with weaker low-k dielectric structures resulting in flip chip becoming narrower in terms of packaging process margin. In addition, there is a big trend in being environmentally friendly, driving lead free and halogen free, or green, material sets. With ultra low-k and interconnects pitch becoming smaller and smaller and with the shift to lead free materials, the technical limitations faced by the packaging industry are becoming more challenging. eWLB technology provides a window for packaging next generation devices in a generic, lead-free/halogen free, green packaging scheme.

Table 1. Advantage of eWLB packaging.

<table>
<thead>
<tr>
<th>Advantage of eWLB packaging.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Thinner &amp; smaller package solution</td>
</tr>
<tr>
<td>2. Ideal for mobile applications and meeting future roadmaps</td>
</tr>
<tr>
<td>3. Package robustness (vs. leadfree flip chip + advanced fab nodes with ELK (extreme low-k))</td>
</tr>
<tr>
<td>4. Cu/low-k compatible packaging technology, Green packaging (Generic Pb-free, Halogen free)</td>
</tr>
<tr>
<td>5. Superior board level reliability proven for mobile applications</td>
</tr>
<tr>
<td>6. Proven lower cost path using a batch process &amp; simpler supply chain</td>
</tr>
<tr>
<td>7. Next generation eWLB technology with 3D eWLB joint development</td>
</tr>
<tr>
<td>8. No substrate or bumping; Simple logistics and supply chain</td>
</tr>
</tbody>
</table>

THERMAL CHARACTERIZATION
Keser et al reported thermal characterization work of chip-embedding technology [3]. Thermal modeling of a 25x25mm 360 I/O with a single 9.9x8.5mm die in a 0.7mm thick mold, powered at 1W, predicted a thermal resistance of 21.4 °C/W in a JEDEC standard natural convection environment.

Understanding the thermal behavior of the embedded package design is beneficial to avoid heating in the structure, while conducting further studies on thermal management solutions show the impact of external cooling aids for additional design considerations.

At the package-level, discrete modeling of the package components are simulated in FloTHERM on a JEDEC standard sized test environment in natural convection [4]. Temperature of the active die’s junction is then inputted into the design parameter of junction-to-ambient thermal resistance, as in equation (1), with a uniform power distribution:

$$\theta_{ja} = \frac{(T_j - T_a)}{P} \quad \ldots \ldots .(1)$$

where,

$\theta_{ja}$- thermal resistance from junction to ambient of package  
$T_j$- die junction temperature  
$T_a$- ambient temperature  
$P$- total power dissipated in the chip

Thermal Performance of eWLB and FI-WLP
Simulations consider parameter of backside protection (BSP) and power dissipation (1.0Watt and 2.0Watt) and compare eWLB and FI-WLP for thermal performance. Table 2 and 3 show details of modeling of eWLB and PCB. As shown in Fig. 3, different package structures are studied for thermal performance. In this study, ambient temperature is set as 70°C. For eWLB, BSP layer is polymer material and it is optional process for packaging
process. eWLB shows as similar thermal performance as FI-WLP and junction-to-ambient thermal resistance, $\theta_{ja}$ is 32 °C/W. As shown in Fig. 4 and Table 4, BSP layer has no significant effect on overall thermal performance. In cases where an external cooling device (heat sink) is applied to the package, the exposed die eWLB will have slightly better thermal heat-dissipation due to direct contact with die backside. The effect of package/mold thickness, with/without heat-sink as well as mold material property would be good parameters to investigate further eWLB thermal performance improvement.

**Table 2.** Specification of eWLB and FI-WLP thermal modeling.

<table>
<thead>
<tr>
<th></th>
<th>eWLB-1</th>
<th>eWLB-2</th>
<th>FI-WLP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Type</td>
<td>212L eWLB</td>
<td>212L eWLB</td>
<td>144L WLP</td>
</tr>
<tr>
<td>PKG Size (mm²)</td>
<td>8x8</td>
<td>8x8</td>
<td>5x5</td>
</tr>
<tr>
<td>Die Size (mm)</td>
<td>5 x 5 x 0.450</td>
<td>5 x 5 x 0.450</td>
<td>5 x 5 x 0.450</td>
</tr>
<tr>
<td>Ball Count</td>
<td>212 I/O</td>
<td>212 I/O</td>
<td>144 I/O</td>
</tr>
<tr>
<td>Ball Pitch</td>
<td>0.50 mm</td>
<td>0.50 mm</td>
<td>0.40 mm</td>
</tr>
<tr>
<td>Ball Diameter</td>
<td>0.28mm</td>
<td>0.28mm</td>
<td>0.28mm</td>
</tr>
</tbody>
</table>

**Table 3.** Thermal properties of eWLB package modeling.

<table>
<thead>
<tr>
<th>Materials</th>
<th>Thermal Conductivity (W/m-K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>120</td>
</tr>
<tr>
<td>Mold Compound</td>
<td>0.88</td>
</tr>
<tr>
<td>Dielectrics</td>
<td>0.30</td>
</tr>
<tr>
<td>Cu RDL</td>
<td>390</td>
</tr>
<tr>
<td>Solderball</td>
<td>55</td>
</tr>
<tr>
<td>Backside Protection</td>
<td>0.12</td>
</tr>
</tbody>
</table>

**Figure 3.** Package modeling schematics of (a) eWLB-1 (with backside protection), (b) eWLB-2 (back-side exposed) and (c) FI-WLP for thermal simulation.

**Figure 4.** Thermal simulation results of (a) eWLB-1, (b) eWLB-2 and (c) FI-WLP

**Table 4.** Thermal performance with cases of Table 2.

<table>
<thead>
<tr>
<th>Power</th>
<th>$1.0 \text{ Watt, } T_{amb} = 70\text{C}$</th>
<th>$2.0 \text{ Watt, } T_{amb} = 70\text{C}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_j (\text{C})$</td>
<td>$\theta_{ja} (\text{C/W})$</td>
</tr>
<tr>
<td>eWLB-1</td>
<td>102.2</td>
<td>32.2</td>
</tr>
<tr>
<td>eWLB-2</td>
<td>102.2</td>
<td>32.2</td>
</tr>
<tr>
<td>FI-WLP</td>
<td>102.8</td>
<td>32.8</td>
</tr>
</tbody>
</table>

**Table 5.** Specification of eWLB and fcBGA thermal modeling.

<table>
<thead>
<tr>
<th></th>
<th>fcBGA-1</th>
<th>fcBGA-2</th>
<th>eWLB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PKG Size (mm²)</td>
<td>11x11</td>
<td>10x9</td>
<td>10x9</td>
</tr>
<tr>
<td>Die Size (mm²)</td>
<td>7.5x7.0</td>
<td>7.5x7.0</td>
<td>7.5x7.0</td>
</tr>
<tr>
<td>Substrate Thickness/Layer</td>
<td>0.18mm / 2-layer</td>
<td>0.18mm / 2-layer</td>
<td>1-layer RDL</td>
</tr>
<tr>
<td>Ball Count</td>
<td>477 I/O</td>
<td>508 I/O</td>
<td>508 I/O</td>
</tr>
<tr>
<td>Ball Pitch</td>
<td>0.50 mm</td>
<td>0.40 mm</td>
<td>0.40 mm</td>
</tr>
<tr>
<td>Ball Diameter</td>
<td>0.3mm</td>
<td>0.28mm</td>
<td>0.28mm</td>
</tr>
<tr>
<td>Backside Protection</td>
<td>-</td>
<td>-</td>
<td>Yes</td>
</tr>
<tr>
<td>PCB</td>
<td>JEDEC standard high effective conductivity PCB (4L)</td>
<td>JEDEC standard high effective conductivity PCB (4L)</td>
<td>JEDEC standard high effective conductivity PCB (4L)</td>
</tr>
</tbody>
</table>

**Figure 5.** Thermal Performance of eWLB and fcBGA

Simulations consider power dissipation (2.0Watt) and different size of fcBGA to compare eWLB and fcBGA for thermal performance with same die size. After design feasibility study eWLB has 46% smaller than fcBGA. Table 5 shows details of modeling of eWLB, fcBGA and PCB. In this study, ambient temperature is set as 50°C. For eWLB, BSP layer is polymer material and it is optional process for packaging process. eWLB shows as similar thermal performance as fcBGA and junction-to-ambient thermal resistance, $\theta_{ja}$ is 21.5 °C/W as shown in Fig. 5 and Table 6.
Figure 5. Thermal simulation results of (a) fcBGA-1, (b) fcBGA-2 and (c) eWLB.

Table 6. Thermal performance with cases of Table 5.

<table>
<thead>
<tr>
<th></th>
<th>Power</th>
<th>$T_j$ (°C)</th>
<th>$\Theta_{ja}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>fcBGA-1</td>
<td>2Watt, $T_{amb} = 50°C$</td>
<td>93.5</td>
<td>21.75</td>
</tr>
<tr>
<td>fcBGA-2</td>
<td></td>
<td>93.6</td>
<td>21.8</td>
</tr>
<tr>
<td>eWLB</td>
<td></td>
<td>93.0</td>
<td>21.5</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERIZATION

High Q Inductor Solution for RF Applications

Inductors are key circuit components for RF applications, which are used in almost all RF functional blocks, such as, LNA, transceiver, power amplifier (PA), filter, balun, etc. The quality-factor (Q-factor) of an inductor is the figure-of-merit for inductor performance.

While high Q solutions from die-level are explored, high Q inductors made from packages are also been brought in the industry for less cost. A typical approach is to make inductors from laminate substrates[5-6]. This approach has been successfully used for RF modules/SiP in PA matching and coupling circuits. Inductors made from a WLP RDL (Redistribution Layer) process are introduced. In this process, the inductors are not sat in the area directly above an active IC, but above some mold compound materials in eWLB through RDL layers. These mold materials mainly serve for two purposes. First, they are actually the package substrates, providing mechanical strength for the respective packages. Second, these mold compounds usually have low loss-tangent, which is essentially a good property for making RF components, such as inductors. Since the inductors are not on top of active ICs, their interferences with active ICs are minimized and signal integrity of ICs may be maintained.

Fig. 6 illustrates an eWLB package, which includes a RF chip, an IPD chip, and RDL inductors above the IPD chip (but not made from the IPD process)[5]. In eWLB package, the connection from the RDL inductors to the RF chip is made through vias connecting the RDL layer and the top metal layer in the RF chip. The connection between the RDL and the IPD chip is made through vias connecting the RDL layer and the top thick metal layer in the IPD. There are three different substrates: CMOS substrate, IPD substrate and mold compound substrate the passivation layers are made through wafer fab process. The measurement was conducted through the G-S-G pads implemented with the inductor. The plotted response includes the contribution from the G-S-G probing pads (not de-embedded).

Fig. 7 depicts Q performance comparison of inductor made from different processes/options. As can be seen, if an inductor is made directly above an active IC through this process, its Q peak is around 26. However, if made in FO area, its peak Q can be 35. Even compared to the same inductor made from regular IPD process [8], the Q value from the inductor made in the mold material is still the best.

The high-Q inductors made in the mold material as eWLB packaging are therefore good candidates for RF passive functional blocks. In addition, the plating Cu RDL process on molded substrate may remove using the specially-treated IPD substrates for low cost. If capacitors are needed in the circuits, we may still use an IPD chip to build them, but the IPD substrate can be regular p-type substrates too for low cost.

Electrical Parasitic Characterization

The RLC parasitic values of eWLB and fcBGA are extracted by computer simulation using commercial 2D electromagnetic field solver. The S-parameter of each packages were extracted by using ANSOFT HFSS. Simulated results are compared with RLC parasitic values and S parameters. Fig.8 shows the package schematics and 3D electrical modeling of fcBGA and eWLB, respectively. These package designs are carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins are selected and studied, such as clock, VDD as well Data pins. Fig. 9 shows comparison of parasitic values of RLC for fcBGA and eWLB at 1GHz. For resistance, eWLB has 68% less value than fcBGA. Moreover, eWLB has 66% less inductance value and 39%
less capacitance compared to fcBGA. It is mainly due to shorter interconnection in eWLB. For fcBGA, there is flipchip solder bump and substrate interconnections all contribute signal delay. eWLB has shorter interconnection with RDL process thus, it has improved electrical performance than fcBGA.

![Figure 8. PKG schematics and electrical modeling of (a) fcBGA and (b) eWLB for electrical simulation.](image)

Table 7 shows RLC value per unit length for fcBGA and eWLB at DC, 100MHz, 1GHz, 5GHz, respectively. Even in unit parasitics, eWLB has less resistance and inductance values than fcBGA at all frequency. As shown in Fig. 10, eWLB shows less reflection noise and better transmission performance than fcBGA over all frequency ranges. fcBGA has the resonance near 7.5–8GHz due to the mutual factor of inductance and capacitance elements. This resonance affects crosstalk of neighbor signal, signal distortion/reflection, power integrity, signal integrity as well as EMI/EMC. But eWLB shows no resonance and better electrical performance so eWLB can be applicable for higher frequency applications.

![Figure 9. Plot of electrical parasitic values of RLC of fcBGA and eWLB @ 1GHz.](image)

### Table 7. RLC value/unit length of total net.

<table>
<thead>
<tr>
<th></th>
<th>fcBGA</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DC</td>
<td>100M</td>
<td>1G</td>
<td>5G</td>
<td>DC</td>
</tr>
<tr>
<td>R</td>
<td>44.38</td>
<td>45.02</td>
<td>92.75</td>
<td>194.01</td>
<td>0.5456</td>
</tr>
<tr>
<td>L</td>
<td>10.08</td>
<td>11.04</td>
<td>21.7</td>
<td>43.5</td>
<td>0.4764</td>
</tr>
<tr>
<td>C</td>
<td>209.6</td>
<td>212.4</td>
<td>425.8</td>
<td>425.8</td>
<td>0.4669</td>
</tr>
</tbody>
</table>

![Figure 10. Plot of S parameter study: Transmission (S21) and Reflection (S11) noise.](image)

### MECHANICAL CHARACTERIZATION

#### Warpage Behavior with Temperature Profile

Among the 3D technologies, Package-on-Package (PoP) is increasingly becoming mainstream due to its flexibility of combination and sourcing. The top package to be stacked using solder ball interconnects. For successful package on package stacking with high assembly yield, warpage of both the top and the bottom package are critical. If the warpage is too large, open solder joints may occur between the bottom package and motherboard, or between the bottom package and top package. Not only is the warpage at room temperature a concern for co-planarity measurement as a control, but warpage at solder reflow temperatures (up to 260°C for lead-free solder) should also be considered since open solder joints occur during solder solidification. As a result, warpage control at both temperature extremes is critical for 3D PoP stacking.

Themo-Moiré technology was used for measure package warpage with temperature profile. There was study of warpage behavior with different materials combinations of dielectrics and molding compound material. 10 samples of each legs were measured with Pb-free reflow profile after solder ball removal.

![Figure 11. Comparison of warpage behavior of eWLB with different material sets.](image)

As shown in Fig.11, warpage behavior is very dependent of materials sets, especially at high temperature. So proper combination of materials are critical to provide stable warpage behavior in eWLB package.
optimized material properties showed very stable warpage behavior in reflow temperature profile.

To compare warpage behaviour with other package type, there were warpage measurement of fcFBGA and eWLB. As shown in Fig. 12, eWLB showed almost flat during temperature profile. But fcBGA package showed serious warpage with direction change. Warpage variation of eWLB was less than 5μm in measured temperature range up to 260°C. This stable warpage behaviour of eWLB is good for fine ball pitch SMT applications as well as PoP or 3D approaches.

Figure 12. Comparison of warpage behavior of various package types; fcFBGA and eWLB with reflow temperature profile.

CONCLUSION
Advanced packaging plays a crucial role in driving products with increased performance, low power, lower cost and smaller form factor. The industry requires innovation in packaging technology and manufacturing to meet current demands and the ability to operate equipment in high volume with large throughput.

eWLB technology is an enhancement to standard WLPs, allowing the next generation of a WLP platform due to its FO capability. eWLB showed improved electrical performance with shorter interconnection length. In comparison to fcBGA, eWLB had less parasitic values of RLC and improved transmission performance as well as less reflection noise. And eWLB had similar thermal performance of FI-WLP and fcBGA.

High Q inductors can be made on top of the eWLB mold compound material, adding value to high performance RF devices. This packaging process is similar to the RDL process in semiconductor industry, which can potentially provide high integration, small-form factor, high yield features for RF products. And eWLB electrical performance was much better than fcBGA because eWLB has shorter interconnection length and it does not have solder bump, substrate via and longer metal lines in substrate. eWLB showed very stable warpage behavior with temperature and it has only ~10um warpage @ room temperature.

eWLB is also low-cost solution with fab inline batch process and larger area utilization such as 12” approaches. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SiP) and 3D stacked packaging. Moreover, 3D eWLB technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of devices as well as 3D TSV integration for true 3D SiP systems.

Electronic product differentiation today is driven by ever-expanding functionality, feature sets, multi-functionality and faster communications. At the same time, consumers have made clear their desires for feature-rich products in compact form factors to enable maximum portability. eWLB technology is successfully enabling semiconductor manufacturers to provide the smallest possible, highest-performing semiconductors as cost-effective packaging solution.

ACKNOWLEDGEMENT
Authors appreciate for support and help from; Won-Joon Ko, Statschippac Korea for Thermo-Moire measurement, and Tae-Huan Jang, Statshippac Singapore, for package design and advice on electrical performance.

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