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Abstract
We have investigated the impact of die thickness on integrated passive device (IPD) performance both in simulation and from measurement for RF stack-die applications. Our simulation approach accurately predicts the behavior of the IPD in such stack-die configuration. This should help us to generate guidelines for RF integrated passive devices to be used in 3D stack-die packages.

Introduction
In RF communication systems, between antennas and transceivers there are switches, filters, baluns, and matching circuits (so called front-end-modules). Traditional implementation of front-end modules (FEM) is to have transceiver packages, and other surface-mount components (for switches and passives, for example) assembled on a system board. A more integrated solution is to use a laminate or LTCC substrate to implement all or some of the above active and passive components in one single package – system in package (SiP).

RF transceivers are mainly made from CMOS technology, while most RF switches are still made from GaAs technology and can not be made along with transceivers for performance reasons. For RF circuits, quality-factors (Q) of passives (inductors, for example) play significant roles in their electrical performance, and therefore passive components (RCL and functional blocks, such as filters and matching circuits) are intentionally made off-chip, through various options from LTCC, laminate, silicon, GaAs or glass substrates[1-4].

While side-by-side approaches are commonly adopted in SiP or MCM applications, stacked-die and 3D wafer-level packaging solutions are attracting attention. 3D assemblies are rapidly evolving into a promising new field, because they may significantly reduce the package footprint and cost by using interconnection through vertical dimension (Z-direction). However, if both chips in a stack-die package have RF functions, either chip can be both aggressor and victim. We have investigated a case, in which the top die is an RF IPD chip and the bottom die is an RF transceiver chip (in flip-chip format) made from CMOS technology. In this study, we examine the case, in which the IPD is a victim impacted by a CMOS chip substrate.

The tested CMOS wafer in the stack-die configuration was selected from a regular p-type CMOS wafer with resistivity of around 1.0 Ohm-cm to 10.0 Ohm-cm. To represent the actual stack-up of the package, the CMOS wafer was facing down with the metal patterns on the bottom side. The IPD wafer was then stacked onto the CMOS wafer for subsequent probing measurement.

Design for Stacked Die Package
1) Silicon IPD Process
In STATS ChipPAC’s silicon IPD process, a specially treated silicon substrate is used to support dielectric layer and metal layers. There are three metal layers (M1, M2, and M3)
and two dielectric layers (PI-1 and PI-2) in the cross section as shown in Figure 1. Layers M1 and M2 are used to form MIM capacitors and their thickness are 1.0 um and 3.0 um, respectively. The capacitance density is 330 pF/mm² from this process. This density is high enough for making capacitors for RF applications (typically less than few tens of pF), but may not be enough for decoupling applications. The layer M3 is made of thick copper, and inductors are implemented in this layer. For RF inductors (typically inductance value less than 30.0 nH), the Q factors achieved from this process are around 25.0 to 35.0, depending on inductance values.

Both wire-bonding and flip-chip type IPDs can be made from this process. Typical finished thickness of the wafer is around 250.0 μm or larger, and the actual circuit elements (RCL) are implemented in the top 10% area of the silicon substrate. With this physical cross section, the Q factor and inductance will be slightly different for an inductor in wire-bonding and flip-chip configurations, which has to be considered in IPD design.

The process tolerance/variation is relatively small, compared to a thick-film (LTCC, for example) technology, which is used for conventional passive components in the industry. Highly repeatable passive circuits (filter, balun, matching, etc) for RF applications can be made through this IPD technology [6-8].

Table I. LC values for the filter components (in pF or nH) and coupling coefficients.

<table>
<thead>
<tr>
<th>L_A</th>
<th>L_B</th>
<th>L_C</th>
<th>C_A</th>
<th>C_B</th>
<th>C_C</th>
<th>k_AB</th>
<th>k_BC</th>
<th>k_AC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.46</td>
<td>2.6</td>
<td>1.1</td>
<td>8.5</td>
<td>1.7</td>
<td>3.6</td>
<td>0.13</td>
<td>0.13</td>
<td>-0.04</td>
</tr>
</tbody>
</table>

The initial LC components based on the values in the table above were created using a GDS tool generator, which complies with the design rules. After some interconnection and a co-planar ground were added to form a functional block, an EM simulation tool was used to simulate the response from the layout. Due to the parasitic and the co-planar ground, the initial EM response altered from the expected response to some extent. Some internal ports were assigned on the electrodes of capacitors for tuning.

The separation/distance between the three inductors used in this device also plays a role in the fine tuning process of its performance. The distances d1, d2 and d3 control coupling strength and therefore the pass-band and stop-band performance. From the circuit topology, the coupling (k_AC) expected response to some extent. Some internal ports were assigned on the electrodes of capacitors for tuning.

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between LA an LC is very weak, and from EM simulation the distance between LA and LC (d3) is not sensitive to this device’s performance. Usually it takes 3-4 iterations to tune the performance back to meet electrical specifications. Detail scheme for designing this BPF can be found in [9].

Design of this device adopts weak coupling scheme between the three inductors. In principle, narrow band response is expected from this device. Due to the symmetric design in layout (Figure 4), the two output ports connecting the two electrodes of the output capacitor (Cc) have almost perfect balanced properties.

The wafer raw thickness is about 750.0 μm before back-grinding. After the IPD wafer was made, probing measurement on the devices above was conducted. Then the wafer was then back-ground to about 425.0 μm (17 mils) and re-measured. Finally, the wafer was back-ground to 150.0 μm thickness. For a small IPD (like a LPF), there is almost no noticeable difference in the pass band performance for thickness variations like these. However, for a large IPD (like this BPF), the performance difference is significant, and is sufficient to make difference between a workable and non-functional IPD. As can be seen in Figure 5, the performance of samples of 420.0 μm and 750.0 μm wafer thicknesses both cover the pass band well. But the performance from the sample of 150.0 μm wafer thickness is impacted negatively, resulting in high insertion loss at the low side of the pass band. It is concluded that this BPF made with 150.0 μm thickness (for example, putting it directly on a laminate substrate) will not have good electrical performance.

In a stack-die packaging scenario, when this IPD is placed over another CMOS die, the electrical characteristics of the CMOS substrate may also have an impact on the IPD performance.

For a typical p-type CMOS wafer used for making RF transceiver, the substrate resistivity is typically in 1.0 Ohm-cm to 10.0 Ohm-cm range. Using the substrate resistivity of this range, we find there is almost no impact on the IPD’s performance. Only when the substrate is nearly conductive (in very low resistivity), it starts to have considerable negative impact on the IPD’s performance (mainly on insertion loss). Figure 6 shows the performance trend with the CMOS substrate resistivity on a BPF (in 150.0 μm thickness) stacked on to a CMOS chip (in 270.0 μm thickness). For the CMOS
wafer resistivity from 1.0 Ohm-cm to 10.0 Ohm-cm, there is no appreciable impact on the IPD’s electrical response. When the silicon substrate resistivity changes from 5.0 Ohm-cm to 0.01 Ohm-cm, the insertion loss at 2.5 GHz degrades from -2.5 dB to -6.5 dB.

Characterization for Stacked Die Package

Wafers with some probable IPDs were made in raw substrate thickness (~750.0 µm). Then they were back-ground to about 420.0 µm, and 150.0 µm thickness. The probing measurements were taken at each wafer thickness level (750.0 µm, 420.0 µm, and 150.0 µm), in order to characterize the IPD’s performance with IPD die thickness.

For the stack-die probing measurement, an IPD wafer in 150.0 µm thickness was used for the top wafer. A CMOS wafer (having resistivity around 1.0 Ohm-cm to 10.0 Ohm-cm) with some metal patterns already deposited was used for the bottom wafer. Figure 7 shows the IPD wafer (in thickness of 150.0 µm, partially cut) sitting on top of a CMOS wafer (in thickness of 270.0 µm) for probing measurement. The IPD wafer was cut to half for the measurement due to some warpage resulted in from the thin IPD wafer (150.0 µm). Tapes were used to stick these two wafers during the measurement. The CMOS wafer was facing down to represent the packaging scenario where a RF transceiver (bottom die) is in flip-chip configuration. The characterization scheme in this paper is summarized in Table II.

<table>
<thead>
<tr>
<th>IPD Thickness (µm)</th>
<th>150 (#1), 420 (#2), 750 (#3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Die Thickness (µm)</td>
<td>270 (metal facing down, #4); 270 (metal facing up, #5)</td>
</tr>
<tr>
<td>#1</td>
<td>IPD thickness effect</td>
</tr>
<tr>
<td>#2</td>
<td>IPD thickness effect</td>
</tr>
<tr>
<td>#3</td>
<td>IPD thickness effect</td>
</tr>
<tr>
<td>#1 + #4</td>
<td>CMOS die effect</td>
</tr>
<tr>
<td>#1 + #5</td>
<td>CMOS die effect</td>
</tr>
</tbody>
</table>

Figure 7 shows the IPD wafer with some probable pads. In this device, there are three inductors. The outer inductor has relatively big size/inner diameter (about 800.0 µm). Theoretically, performance of a larger inductor is more impacted by a ground plane location than a smaller inductor. But quantitative analysis can be only obtained from EM simulation or experiment.

Figure 8 is a micrograph of the BPF. The intrinsic size of the IPD (excluding the G-S-G probing pads) is about 2.0 mm x 1.2 mm. From the measurement data (Figure 9), at 420.0 µm and 750.0 µm die thicknesses, the performance is almost identical. But at 150.0 µm die thickness, the low side of the pass band response is deteriorated very much, and unacceptable insertion loss is seen. In other words, the IPD in 150.0 um thickness alone does not have good response. This validates the trend obtained from simulation.

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The 150.0 μm thick IPD (wafer) was then stacked onto a CMOS chip (wafer). The CMOS wafer had been back-grinded to about 270.0 μm. Therefore the ground plane for the IPD inductors is about 150.0 + 270.0 = 420.0 μm. Figure 10 shows the results of this BPF in the stacked configuration. Importantly, the 150.0 μm thick IPD, once being staked onto a CMOS die (in 270.0 μm thickness), retrieves its good behavior as this IPD being 420.0 μm thick alone.

Another test was also conducted to see the effect when the bottom die (wafer) was facing up, which application could be represented by a wire-bonding CMOS die (bottom die) in a stack-die package. The electrical response from both facing-up and facing-down configurations for the bottom die is depicted in Figure 11 for comparison. As shown in this figure, the difference between these two cases is significant (more than 1.5 dB insertion loss difference!). The response from the lower side of the pass-band is severely impacted, mainly due to the presence of the metal patterns on the bottom CMOS die. It is concluded that the bottom die configuration (either wire-bonding or flip-chip) should be taken into account in early packaging design stages, and simply using the IPD design of flip-chip for wire-bonding configuration, or vice versa, would not achieve the expected electrical response.

Besides experimental characterization, we have also simulated the IPD’s electrical performance. In Figure 12, simulation and measurement for the BPF with 420.0 μm
thickness is compared. Excellent agreement between simulation and measurement is achieved. Simulations with other parameters, such as IPD die’s thickness and CMOS die’s presence are also carried out, and they all have good agreements with the measurement.

Conclusions

Several IPD candidates on the wafer of 150.0 µm thickness were used for this stack-die packaging characterization. For some small IPDs in size less than 1.0 mm x 1.0 mm, such as LPF and balun, we found that the thickness of the CMOS die (bottom die) makes no appreciable difference on IPDs’ electrical behaviors. However, for some large IPD (2.0 mm x 1.2 mm, for example) with large inductor coils, the CMOS die thickness does have a noticeable impact on the IPDs’ performance, resulting in characteristics ranging from workable to failed against the specifications.

In a stack-die package design, the elevation (distance to GND) of IPD inductors has to be taken into account, and a budget arrangement of package height in early design stages may be needed for IPDs with large inductor coils used in such stack-die package.

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References