STATSChipPAC®

SPM-E

Simplified Package Modeling - Electrical

Why Perform Full Package Electrical Simulation?

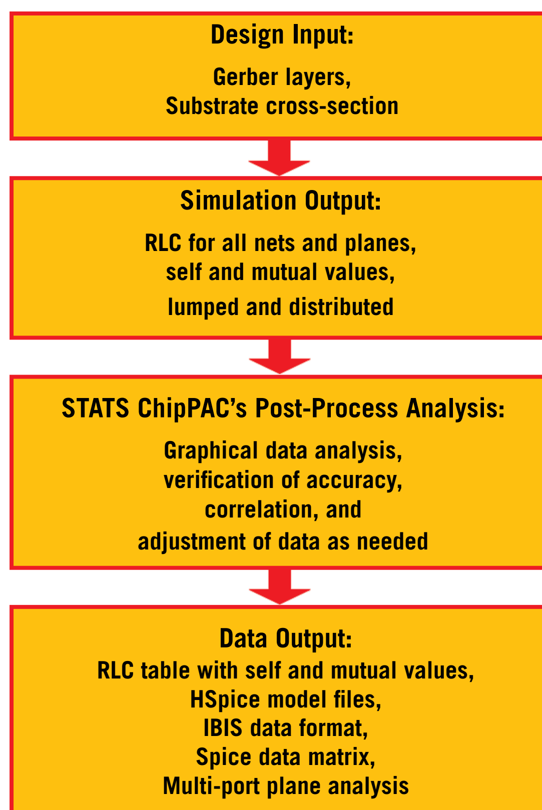
The purpose of full package electrical simulation is to predict the electrical parasitics (RLC) for every net and plane in a specific package design. Understanding and controlling the electrical parasitics greatly enhances the chances that a complex IC will function properly in its application. Electrical simulation requires a minimum lead time when compared with experimental testing because sample parts are not required. Accurate and timely simulation results can reduce the need for subsequent design changes and/or delays.

Simplified Package Model - Electrical

Predicting IC electrical performance and functionality after it has been packaged is a key challenge for packaging engineers. STATS ChipPAC has developed a leading-edge approach to full package electrical characterization called Simplified Package Modeling–Electrical (SPM-E) that provides customers with early and accurate confirmation of electrical performance for the entire design. SPM-E allows full package electrical characterization for all types of leaded and array IC packages including PBGA, EBGA, CSP, multi-chip modules, and stacked die packages.

SPM-E consists of two major steps – simulating the entire design using a quasi-static electrical simulation tool and then post-processing the resulting data to verify and improve accuracy. The STATS ChipPAC post-processing step makes use of graphical analysis to check the data distribution for the entire package. The normalized data distributions are correlated with experimental results from the STATS ChipPAC electrical database and other sources. For specific data components, pre-defined adjustments are applied, based on the expected behavior of the appropriate package type. Using this process, SPM-E has consistently provided accurate results with minimum lead time. Results for leaded packages and small array packages are delivered to the customer within 0.5 to 2 days of receiving the initial design; very large BGA designs take slightly longer.

SPM-E Process Flow



Data Output Formats

Another advantage of SPM-E is the variety of data output formats that are possible. The most general format is a data table that contains the self RLC values and the highest mutual RLC value for every net and plane. These can be separated into values for each component of the circuit (wire, trace, solderball, etc.) as needed by the customer.

The data can also be reformatted as requested by the customer: HSpice, IBIS format, and Spice matrix format for use with customer specific equivalent circuit models.

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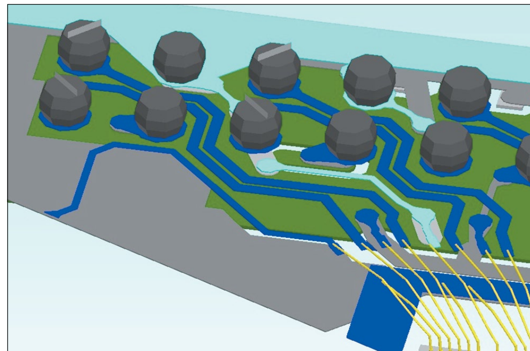
Summary

Since implementing the SPM approach in early 2002, STATS ChipPAC has been able to provide unique benefits to our customers including:

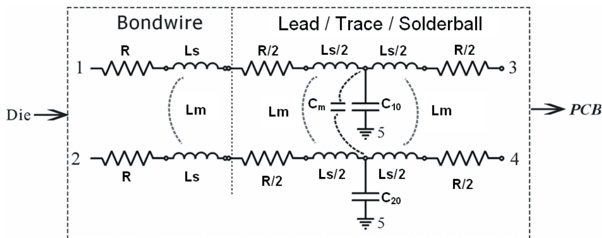
- Accurate and consistent RLC data to customers on average 1 to 3 days from receipt of design drawings.
- Full package simulation of leaded, PBGA, EBGA, CSP, stacked die and MCM packages regardless of size and complexity.
- Customer data provided in various formats as required: distributed RLC, lumped RLC, IBIS, HSpice.

Correlation Example



3.125 Gbs Design

Equivalent Circuit Example



Equivalent Circuit Using Distributed RLC Data

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