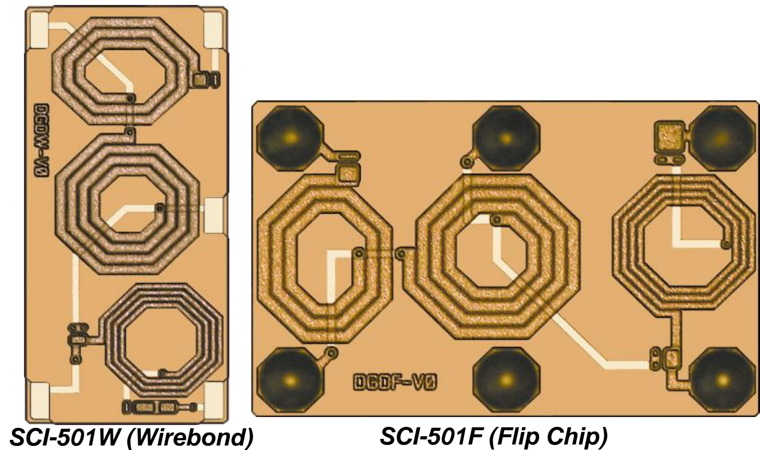
(27) GSM-DCS Diplexer (SCI-501 W/F)

FEATURES

- Passive integration on silicon substrate
- Low insertion loss in pass band
- Small size: 2.1 mm x 1.0 mm (wirebond)
  2.0 mm x 1.3 mm (flip chip)
- Pb-free solder bump
- Low profile: 0.25 mm height (wirebond)
  0.40 mm height (flip chip)
- Directly attachable on PCB or flipped on PCB
- Operating temperature: -40℃ to +85℃
- Storage temperature: -40℃ to +85℃



SCI-501W (Wirebond) *SCI-501F (Flip Chip)*

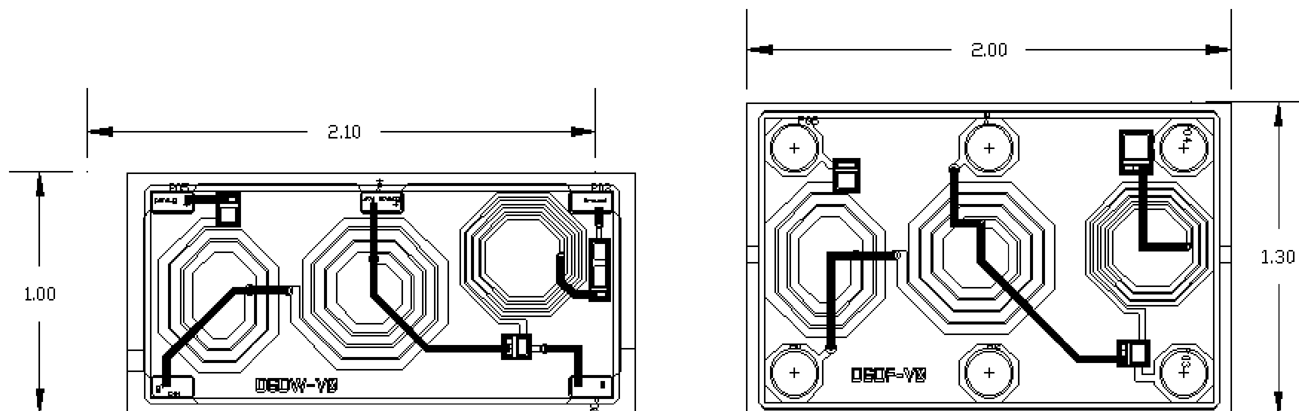
DESCRIPTION

STATS ChipPAC's SCI-501W/F is a diplexer for GSM/DCS band applications. The diplexer has low pass–band insertion loss and small size. It is composed of thick copper inductors and Metal-Insulator-Metal capacitors which are fabricated on a silicon substrate using our IPD (Integrated Passive Device) process. The pad or bump size and pitch of the diplexer are selected so that the device can be mounted directly on a PCB or laminate substrate using conventional wirebonding or surface mount techniques. The low profile and small form-factor of the device make it especially suitable for SiP applications.

ELECTRICAL SPECIFICATIONS

Specification	Unit	Min.	Typical	Max.
Pass Band 1	MHz	824		915
Pass Band 2	MHz	1710		1980
Insertion Loss, Band 1	dB		0.5	
Insertion Loss, Band 2	dB		0.8	
Return Loss, Band 1	dB		20	
Return Loss, Band 2	dB		15	
Isolation, Band 1 at Band 2	dB		20	
Isolation, Band 2 at Band 1	dB		25	
Size	mm	2.1 x 1.0 (WB)		2.0 x 1.3 (FC)

DIMENSIONS



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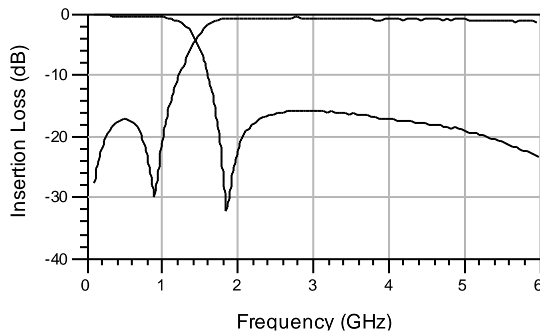
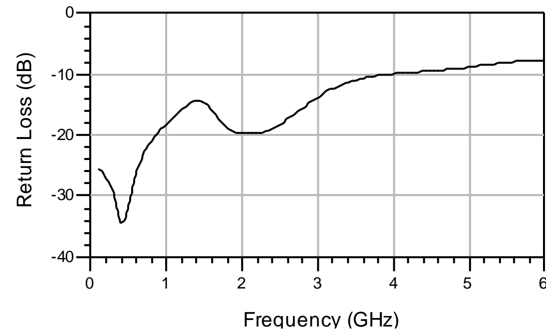
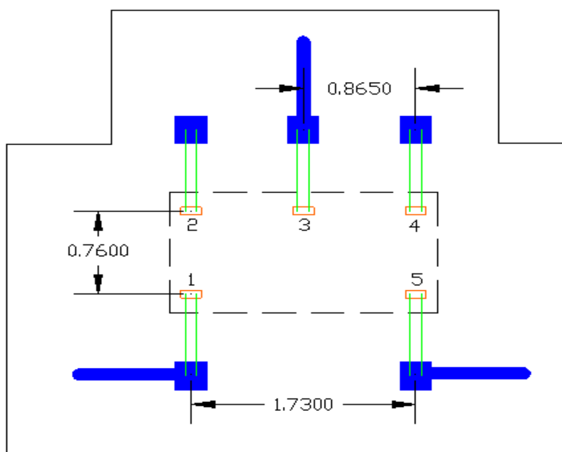
TYPICAL CHARACTERISTICS



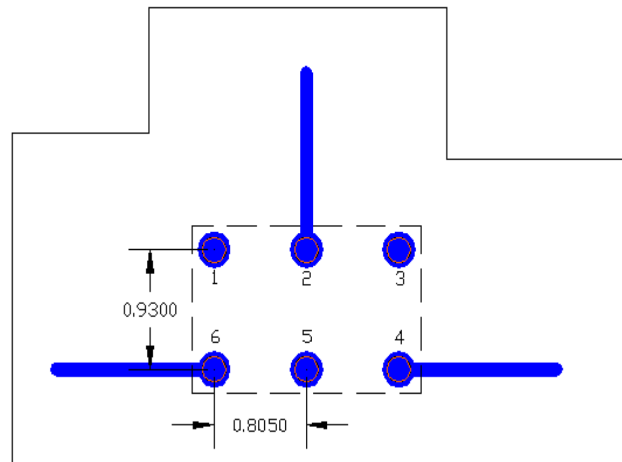


ASSEMBLY DRAWING / MECHANICAL OUTLINE

SCI-501W (Wirebond)



SCI-501F (Flip Chip)



Pad	SCI-501W Signal	SCI-501F Signal
1	Output-1 (Pass Band 1)	Ground
2	Ground	Input
3	Input	Ground
4	Ground	Output-1 (Pass Band 1)
5	Output-2 (Pass Band 2)	Output-2
6	-	Output-2 (Pass Band 2)

NOTES

All dimension measurement units are in millimeters (mm). Electrical performance and typical values are measured at room temperature. For best results, ground plane directly beneath the device should be in the top metal layer.

Refer to “Appendix A” for:

- Pad sizes and typical wirebond length used in the wirebonded IPD products.
- Recommended solder thermal profile, landing pattern recommendation and bump specifications used in the flip chip IPD products.

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