Flip Chip FBGA (fcCSP)

fcFBGA, fcLGA, fcPoP-MLP, Bare Die fcPoP, fcFBGA Hybrid

HIGHLIGHTS

• A complete portfolio of high to low-end fcCSP packages for all mobile applications, including fcFBGA, fcLGA, flip chip package-on-package (bare die PoP and molded laser PoP) and hybrid flip chip/wirebond solutions
• A leader in the development of a broad range of low cost substrate and process technologies for the cost sensitive mobile market
• Ultra low flip chip interconnect parasitics eliminates wire inductance and resistance compared to wirebond interconnect
• One piece heat spreader can be added for exceptional thermal performance

FEATURES

• Body sizes 4 x 4mm through 17 x 17mm
• Electroplated Eutectic SnPb, hi-Pb or Pb-free bumps or Cu column
• Bumping capability down to 130µm pitch with lead-free solder and pitch down to 40µm with Cu column
• Full service wafer bumping with BCB and Polyimide dielectric options for wafer repassivation and redistribution layer (RDL)
• Molded underfill (MUF) or Capillary underfill (CUF) options
• Uniquely developed fcCuBE MR process supports bump pitches down to 80µm and below, providing a lower cost alternative to TCB
• Thermal-Compression Bonding with Non-conductive Paste (TCNCP) available
• MUF with solder bump and Cu column qualified and in production
• 0.40mm min. package ball (BGA) or pad (LGA) pitch in production
• 145µm minimum die solder bump pitch in production
• BGA pitch down to 0.35mm qualified and in production
• Maximum overall height of 1.40mm (fcLFBGA); 1.20mm (fcTFBGA); 1.00mm (fcVFBGA); 0.65mm (fcLGA)
• Conventional 2 to 6 layer through-hole or PPG build-up laminate substrates available; ABF build-up substrates available
• Low cost substrate technology options including Embedded Trace Substrate (ETS) in HVM, and Via Under Trace (VUT) qualified, No-Clean Flux and Non-PI Bumping qualified or HVM, and others such as large die CUF and Land Side Cap (LSC) with 0.4mm BGA pitch in development
• One piece heat spreader option for exceptional thermal performance; fcFBGA-ED-H (1-piece heat spreader) with MUF qualified
• Packages assembled in either bare die, exposed die and overmolded strip matrix format, and saw singulated; high density wide strip available

DESCRIPTION

STATS ChipPAC’s fcFBGA packages form a subgroup of the Flip Chip package family of the form factor known as Chip Scale Packages (CSP). STATS ChipPAC offers a complete fcFBGA portfolio of high to low-end leading edge packages for all mobile applications including standard fine pitch fcFBGA packages, hybrid flip chip and fcPoP including Bare Die fcPoP and Molded Laser PoP (fcPoP MLP).

STATS ChipPAC’s fcFBGA packages offering includes very thin profile packages (fcTFBGA, fcWFBGA and fcUFBGA), as well as side-by-side die configurations. All fcFBGA packages are produced on substrates with matrix strip format and use overmolding and saw singulation processes similar to wirebond packages of the same form factors. The fcFBGA is an overmolded package with solder balls, and is available in a high thermal performance package (fcFBGA-H) produced on substrates in matrix strip format with heat spreader.

fcFBGA packages are also available in very thin profile hybrid flip chip (flip chip on the bottom and wirebond die on the top) such as fcTFBGA-SD2 and fcTFBGA-SD3. Hybrid fcFBGA packages are available with Mass Reflow (MR), CUF or MUF, and copper (Cu) pillar and Cu wire.

STATS ChipPAC’s fcFBGA offering also includes package-on-package (PoP) solutions in Bare Die and Molded Laser formats. Both fcPoP formats are offered as the bottom PoP package (PoPb) of a stackable flip chip BGA. PoPb is typically an application processor or an integrated baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a second FBGA or PoP top (PoPt) above.

Bare Die PoP differs from fcFBGA through the inclusion of memory interface (MI) pads on the substrate top side. Molded Laser PoP (MLP) offers aggressive package height reductions or 0.35mm MI pitch, and, with its overmold configuration, provides better warpage performance. MLP-PoP is also offered with an exposed die (ED) which reduces mold cap height and improved warpage performance.
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**Applications**

STATS ChipPAC offers a complete fcFBGA portfolio of high to low-end packages for all mobile applications:

- **Mobile processors for Smart Phones, Tablets and Wearable Electronic (WE) devices including baseband, application processors, and application processors + baseband**
- **Chipsets for peripheral IC’s driven by demand for high-end Smart Phone functionality, including RFIC, PMIC, Connectivity, Sensors/ MEMS, and Audio CODEC**

**THERMAL PERFORMANCE**

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

<table>
<thead>
<tr>
<th>Package</th>
<th>Body Size (mm)</th>
<th>Pin Count</th>
<th>Die Size (mm)</th>
<th>Thermal Performance θ°C/W</th>
</tr>
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<tbody>
<tr>
<td>fcFBGA</td>
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<td>191</td>
<td>4.46 x 5.65</td>
<td>33.2</td>
</tr>
<tr>
<td>fcFBGA-H</td>
<td>14 x 14</td>
<td>425</td>
<td>4.9 x 4.9</td>
<td>14.0</td>
</tr>
<tr>
<td>fcLGA</td>
<td>13 x 13</td>
<td>144</td>
<td>5.5 x 5.5</td>
<td>27.7</td>
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<td>3.8 x 5.0</td>
<td>35.6</td>
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Notes: Simulation data for package mounted on 4 layer PCB (per JESD51-1) under natural convection as defined in JESD51-2. *H/S: 0.3mm formed “Hat” type; 100um TIM1 and 100um lid adhesive: 1.75W/mK.

**Electrical Performance**

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a fcFBGA package, body size 13 x 13mm, 6.0 x 8.0mm die size and frequency of 100MHz.

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**Cross-Sections**

- **fcFBGA**
  - Market: Smart Phone & Tablets AP+BB processors and BB; Chipsets (RFIC, PA, XCVR, PMIC, Connectivity, etc)
  - fcFBGA
    - Very thin profile package
  - fcFBGA-SS2
    - Very thin profile, 2 die side by side package
  - fcFBGA-ED-H
    - Fine pitch, exposed die with heat spreader
- **fcFBGA-PoP**
  - Very thin profile, bare die PoP
- **fcFBGA-MLP PoP**
  - Very thin profile, molded laser PoP
- **fcFBGA MLL PoP-ED**
  - Very thin profile, molded laser, exposed die PoP

**Reliability**

- **Moisture Sensitivity Level**
  - JEDEC Level 3 @ 260°C
- **Temperature Cycling**
  - -55°C/125°C, 1000 cycles (typical)
- **High Temperature Storage**
  - 150°C, 1000 hrs (typical)
- **Unbiased HAST**
  - 130°C, 85% RH, 2 atm, 96 hrs (typical)

**Specifications**

<table>
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<th>Die Thickness</th>
<th>Minimum Bump Pitch</th>
<th>Marking</th>
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<td>0.65 – 1.4mm</td>
<td>250μm – 80μm</td>
<td>130μm, Lead-free solder</td>
<td>Laser</td>
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**Hybrids**

- **fcFBGA-Hybrid w/CUF**
  - Very thin profile hybrid Wirebond – Flip Chip
- **fcFBGA-Hybrid Fine Pitch Cu Column**
  - Very thin profile hybrid Wirebond – Flip Chip
- **fcFBGA Hybrid-SS2, Cu wire**
  - Very thin profile, 2 die side by side, stacked hybrid