eWLB (FOWLP Technology)

Embedded Wafer Level Ball Grid Array

STATS ChipPAC offers a high performance fan-out wafer level packaging (FOWLP) solution that provides significant bandwidth, performance, form factor and cost benefits compared to other packaging technologies available today.

Proven Leadership in Innovative FOWLP Solutions

- Versatile FOWLP platform for advanced system level integration
- Highest integration density commercially available in the industry today
- Flexibility to integrate die from diverse processes, manufacturing sources & silicon wafer nodes for increased functionality
- Excellent mechanical, electrical & thermal performance
- Effectively accommodates new lithography nodes
- Flexible, cost effective 2D, 2.5D & 3D solutions across a broad range of market segments & applications

FEATURES

PERFORMANCE
- Unprecedented flexibility in 2.5D & 3D integration with Si partitioning capabilities
- Advanced dielectric materials for highly reliable, power-efficient solutions
- Strong electrical performance (capable to beyond 60GHz)
- Highly effective heat dissipation for strong thermal performance
- KGD process helps achieve strong yields (99.9%)

FORM FACTOR
- Maximum I/O density; 1.5-2X increase in routing density in the smallest, thinnest footprint commercially available today
- Thin film processing enables very fine lines for X,Y routing (line-width/line-space ratios <10µm/10µm), very fine via pitches & thin dielectrics
- Die-to-die, die-to-passives, & passives-to-passives placement distances below 100µm
- Fine pitch copper (Cu) column bumps provide tighter pitch for 2.5D/3D designs
- Industry's thinnest 3D PoP solutions (ultra thin z-height of 0.3mm with stacked thickness down to 0.8mm height)

COST
- Well established, high volume manufacturing process enables scaling devices to larger panel sizes for compelling cost reduction
- Thin film interconnection offers lowest cost structure over competing advanced manufacturing approaches
- Elimination of substrate results in a thinner package with lower warpage, simplifying supply chain & reduces costs
- 2.5D and 3D options offer a more cost effective & infrastructure-friendly alternative to expensive TSV integration

A breakthrough technology, embedded Wafer Level Ball Grid Array (eWLB) is a versatile fan-out wafer level packaging platform (FOWLP) designed to address the growing mismatch in interconnect gap, higher levels of integration, improved electrical performance and shorter vertical interconnects. The eWLB platform provides a more space-efficient package design enabling a smaller footprint, higher density input/output (IO) and lower package profiles.

Assembled directly on a silicon wafer, this FOWLP approach is unconstrained by die size, providing the design flexibility to accommodate an unlimited number of interconnects between the package and the application board for maximum connection density, finer line/spacing, improved electrical and thermal performance and small package dimensions to meet the relentless form factor requirements and performance demands of the mobile market.

eWLB's flexible manufacturing process can reduce substrate complexity and costs while achieving very dense interconnection in a range of reliable, low-warpage 2D, 2.5D and 3D solutions including small die, large die, stacked or side-by-side multi-die and ultra-thin options across a broad range of market segments and applications.

The basic structure of eWLB, thin film processing, has enabled STATS ChipPAC to create eWLB-based interposers that can connect one active die to another, enabling very dense interconnection with more effective heat dissipation, improved processing speed and the flexibility to integrate die from different manufacturing sources. The result is a proven 2.5D solution that is superior to TSV in terms of overall cost effectiveness and process simplicity.

STATS ChipPAC's 3D SiP and PoP solutions include embedded multiple passives and active components, face-to-back or face-to-face options, and single-sided, 1.5-sided and double-sided ultra-thin PoP configurations. For applications requiring full 3D integration, STATS ChipPAC's face-to-face (marsupial) eWLB PoP configuration provides a direct vertical interconnection between an application processor die and a memory die through the eWLB mold layer to enable a high bandwidth, very fine pitch structure with performance that parallels TSV technology.
eWLB (FOWLP Technology)

Embedded Wafer Level Ball Grid Array

APPLICATION SPACE for FOWLP

When determining the optimal platform among the space of device I/O densities and product architectures, early stage co-design helps ensure the lowest cost solution. As the gap between chip I/O and PCB density increases, STATS ChipPAC has analyzed the fan-out ratio of different package designs and identified the “sweet spot” for eWLB.

RELIABILITY

COMPONENT LEVEL RELIABILITY

- Moisture Sensitivity Level
- Temperature Cycling (after precon)
- Unbiased HAST
- High Temperature Storage
- Temperature Humidity Bias Test
- High Temperature Operating Life
- Multiple Solder Reflow

BOARD LEVEL RELIABILITY

- Temperature Cycling on Board
- Drop Test
- Bend Test
- Temperature Humidity Bias Test

THERMAL PERFORMANCE (θja (°C/W))

Thermal performance is highly dependent on package size, die size, substrate layers and thickness and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

eWLB PROCESS FLOW

1) Reconstituted wafer
- Wafer saw and pick-and-place from incoming wafer
- Probed good die
- Molded reconstituted wafer using proven materials
- Molded artificial wafer starting point for thin film technology

2) Redistribution
- Thin film technology with advanced design rules
- Standard thin film equipment
- Proven and reliable material set

3) Ball Mount and Singulation
- Standard back-end assembly flow (and equipment)

SPECIFICATIONS

Package Thickness
0.4mm - 0.6mm
Bump Pitch
0.3mm minimum
Bump Height
0.2mm / 0.23mm (0.4mm / 0.5mm pitch)
Backside Coating
Laminated coating (optional)
Marking
Laser marking
Inspection
Automatic optical inspection w/ electronic wafer mapping
Packing Options
Fully automated die pick/place into custom pocket tape/reel or waffle pack media

eWLB PRODUCTS PORTFOLIO

- The most comprehensive FO portfolio in the industry
- Wide range of small die, large die, flip chip, stacked or side-by-side multi-die & ultra-thin options
- Body sizes: 2.2 x 2.2mm–14 x 14mm & expanding (package size dependent on die size)
- 2D solutions in single & multi-die configurations down to 0.4mm
- 2.5D eWLB interposer solutions (replaces stacked package configurations or to enable 3D TSV)
- 3D SiP & PoP solutions include embedded multiple heterogenous passives & active components, face-to-back or face-to face options & single-sided, 1.5 & double-sided PoP configurations (total stacked PoP height < 1.0mm)
- MCP versions with flip chip & IPD integration capability