The Market Leader in eWLB Technology

As the world demand for portable electronics accelerates, the need for more sophisticated, high performance semiconductors in a smaller package size has never been greater. Consumers are looking for portable devices with the most features and functionality in the smallest size and lowest cost possible. STATS ChipPAC offers advanced, leading edge wafer level packaging and test solutions for a wide range of mobile applications.

**What is eWLB technology?**

Embedded Wafer Level Ball Grid Array (eWLB) is a powerful Fan-out Wafer Level Packaging (FOWLP) technology with the design flexibility to accommodate an unlimited number of interconnects, unconstrained by die size. This enables eWLB to deliver maximum connection density, improved electrical and thermal performance and small package dimensions to meet the relentless form factor requirements and performance demands of the mobile market.

STATS ChipPAC is a leader in this versatile, cost effective technology platform which integrates semiconductor die from diverse semiconductor processes and silicon nodes. As advanced fab technology nodes drive smaller silicon die sizes with finer interconnect pitches, eWLB offers the scalability to support higher performance, higher bandwidth and lower power consumption requirements in portable and mobile devices by enabling smaller fan-out packaging designs with finer line/spACING, improved electrical performance and passive embedded capabilities.
The eWLB advantage

eWLB technology provides significant performance, size and cost benefits compared to other packaging technology available today. Benefits include:

- Breakthrough super thin packaging options
- A dramatically higher number of input/output count compared to fan-in wafer level packages
- Robust package platform with strong thermal and electrical performance offering a high performance, power-efficient solution
- Scalable heterogeneous die integration capability
- Ability to embed multiple active and passive components in the same wafer level package with a vertical 3D interconnection that can be achieved without TSV
- Established supply chain and proven manufacturing processes for cost-effective solutions across a broad range of market segments and applications

Cost-effective wafer level manufacturing

STATS ChipPAC’s automated eWLB manufacturing process—wafer reconstitution, wafer level molding, redistribution using thin film technology, solder ball mount, package singulation and testing—has proven to be a solid foundation on which STATS ChipPAC has led the industry in a number of technology and manufacturing milestones including:

- First to achieve high volume eWLB manufacturing with best-in-class yields
- First to implement eWLB wafer manufacturing capabilities on larger 300mm reconstituted wafers, achieving higher efficiencies and economies of scale for a more cost effective solution
- First to introduce innovative eWLB designs such as side-by-side devices embedded in a package, package-on-package and ultra thin eWLB packages

STATS ChipPAC is an industry leader in driving yield, throughput and cost-effectiveness of this innovative advanced FOWLP technology.

The 300mm advantage

With more than twice the packages of a 200mm wafer, the 300mm eWLB wafer offers high performance at a lower cost.
A versatile platform for 2.5D and 3D integration

Increasing demand for more advanced, smaller and lighter mobile products with superior functionality and lower overall cost is driving the development of more innovative and sophisticated packaging technologies. STATS ChipPAC has leveraged eWLB technology to drive substrate simplification and cost reduction while achieving tighter line/spaces in a range of 2D to 2.5D and 3D configurations that deliver product advantages to our customers in terms of higher performance, higher frequencies, higher bandwidth and thinner package profiles.

With the inherent performance and cost advantages of eWLB, STATS ChipPAC is also effectively addressing some of the challenges in high end Flip Chip applications that require much finer bump pitches, higher input/output densities and the elimination of stress on extreme low-k or ultra low-k (ELK/ULK) dielectric structures at advanced silicon wafer nodes. eWLB’s fan-out packaging approach with its fine line width and spacing, inherently lower stress, larger pad pitch, and redistribution layer (RDL) allows higher integration and routing density in less metal layers in an fcBGA substrate.

2.5D integration

With advanced eWLB technology, customers have the flexibility to integrate die from diverse semiconductor processes and different silicon nodes into a cost effective 2.5D interposer solution. STATS ChipPAC’s eWLB based interposers enable very dense interconnection with more effective heat dissipation and improved processing speed in a proven, low-warpage packaging structure.

The simplified materials supply chain and lower overall cost available with an eWLB based interposer provide a strong technology platform and path for customers to transition their devices to more advanced 2.5D and 3D packages.

3D integration

eWLB provides the flexibility to embed multiple active and passive components in the same wafer level package with a vertical 3D interconnection that can be achieved with or without the use of Through Silicon Vias (TSVs).

STATS ChipPAC’s eWLB PoP solutions are available in either a single or double-sided configuration and provide a flexible integration platform for stacking a wide range of memory packages on top with a final stacked package height below 1.0mm, and can accommodate up to 1024 interconnections between the memory and processor die. The double-sided eWLB PoP technology features a flexible redistribution layer that can accommodate multiple active or passive devices in complex 3D SiP structures which enable very thin profiles, increased performance and superior warpage control.

With its continuous innovation and extensive manufacturing experience in eWLB technology, STATS ChipPAC provides a flexible integration platform for 2.5D and 3D packaging at a lower overall cost with proven solutions that address advanced wafer fab nodes and the semiconductor industry’s rapid technology evolution.
Ideal applications for eWLB

With its many technology attributes, including a solid integration platform and a revolutionary structure making it one of the thinnest package profiles in the industry, eWLB appeals to an increasingly broad range of market applications in wireless connectivity, networking, microcontroller, power management, storage, embedded and automotive applications. eWLB is successfully supporting mobile applications in devices such as:

- Application Processors / Baseband
- RFIC / RF Transceivers
- WiFi Combo Chips / GPS
- Power Management ICs
- Wireless Local Area Networks
- Micro Controller Units
- CMOS PA / Modules

Although typical package sizes have been in the 2mm to 8mm range, ongoing development activities in eWLB technology is expanding the size range up to 14mm.

Learn more

eWLB technology is rapidly becoming the wafer level packaging solution that more customers are choosing for complex and power efficient semiconductor devices in mobile phones and other handheld electronic products.

To find out more about eWLB, visit us online at www.statschippac.com/eWLB

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